芯动力——硬件加速设计方法

第五章 静态时序分析(1)

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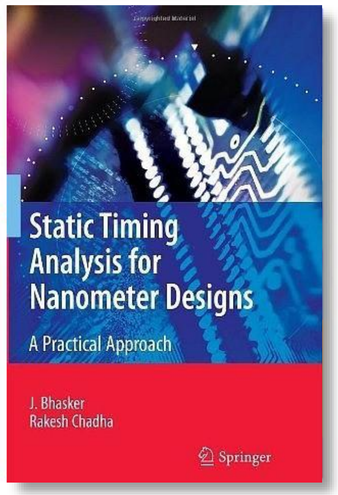
参考教材章节

- Rakesh ChadhaJ. Bhasker. Static Timing Analysis for Nanometer Designs. Springer, 2009. Chapter-8.



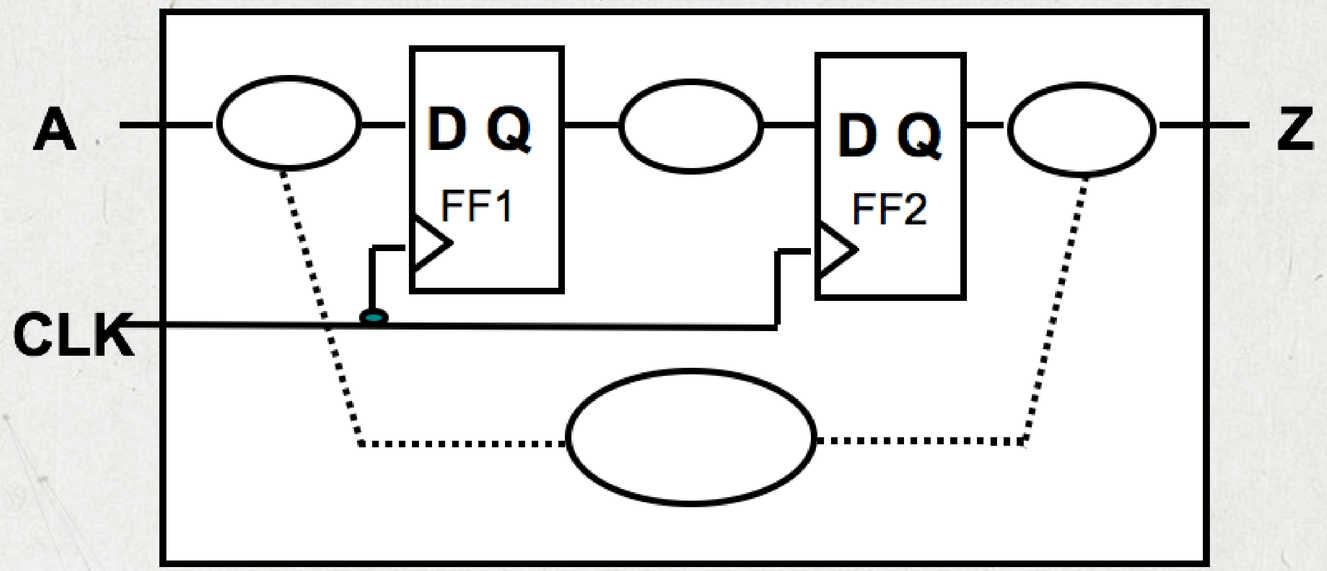
Static Timing Analysis for Nanometer Designs

A Practical Approach

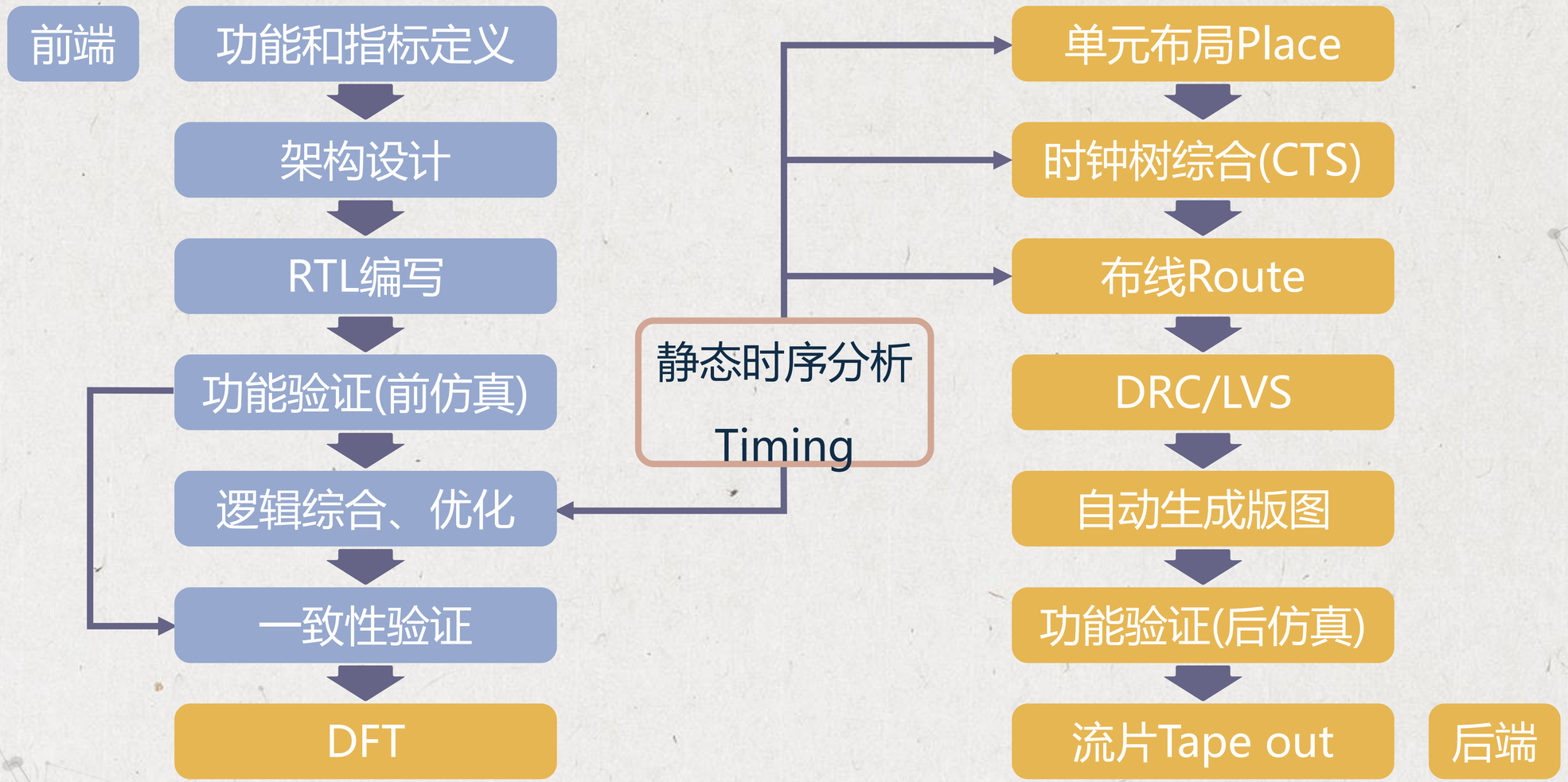
Authors: **Bhasker**, J., **Chadha**, Rakesh

What Is Static Timing Analysis?

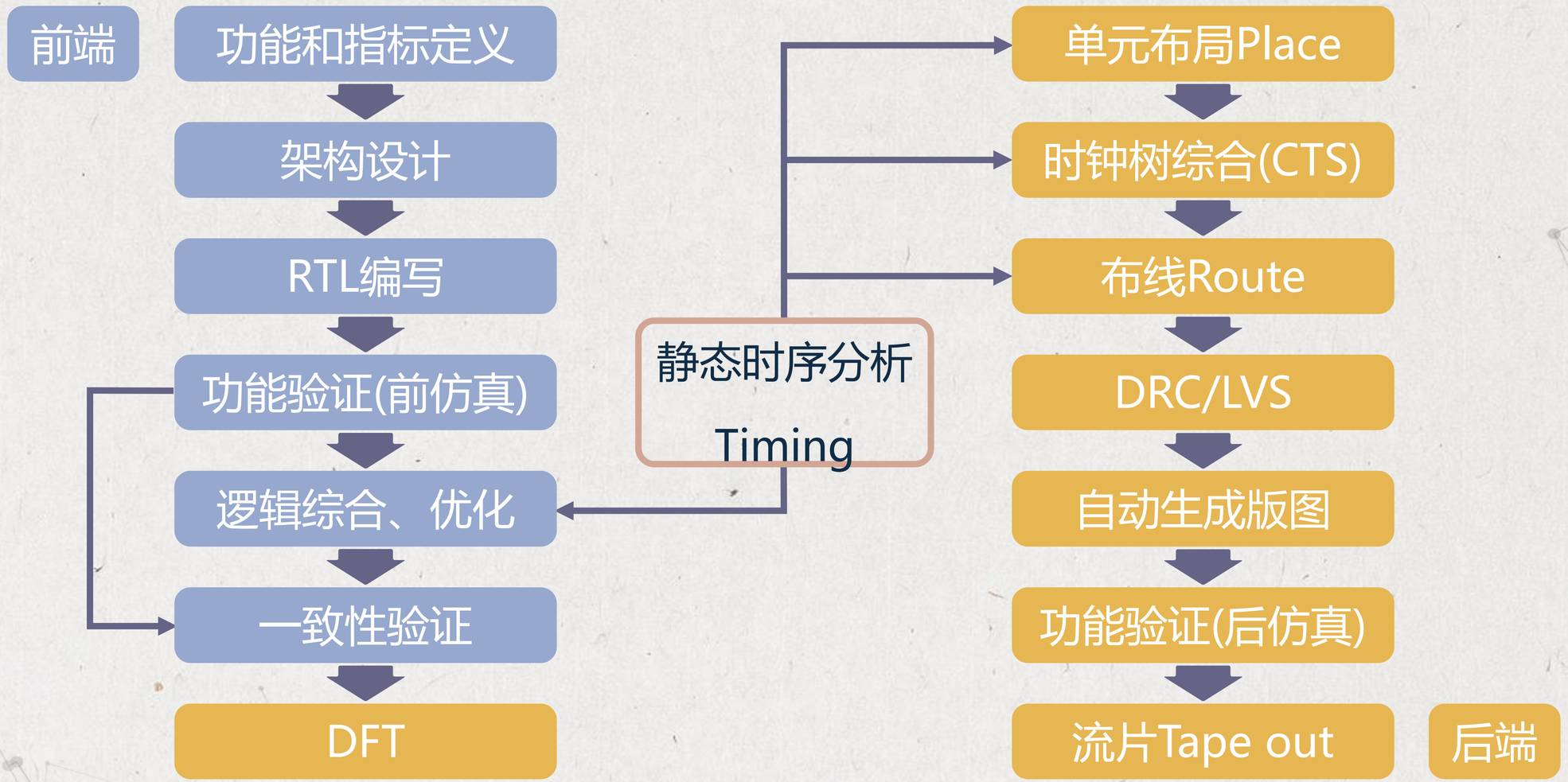
- Static Timing Analysis is a method for determining if a circuit meets timing constraints without having to simulate:
  - Much faster than timing-driven, gate-level simulation
  - Proper circuit functionality is not checked
  - Vector generation NOT required



回顾：芯片设计流程


前端
功能和指标定义
架构设计
RTL编写
功能验证(前仿真)
逻辑综合、优化
一致性验证
DFT
静态时序分析
Timing
单元布局Place
时钟树综合(CTS)
布线Route
DRC/LVS
自动生成版图
功能验证(后仿真)
流片Tape out
后端

回顾：芯片设计流程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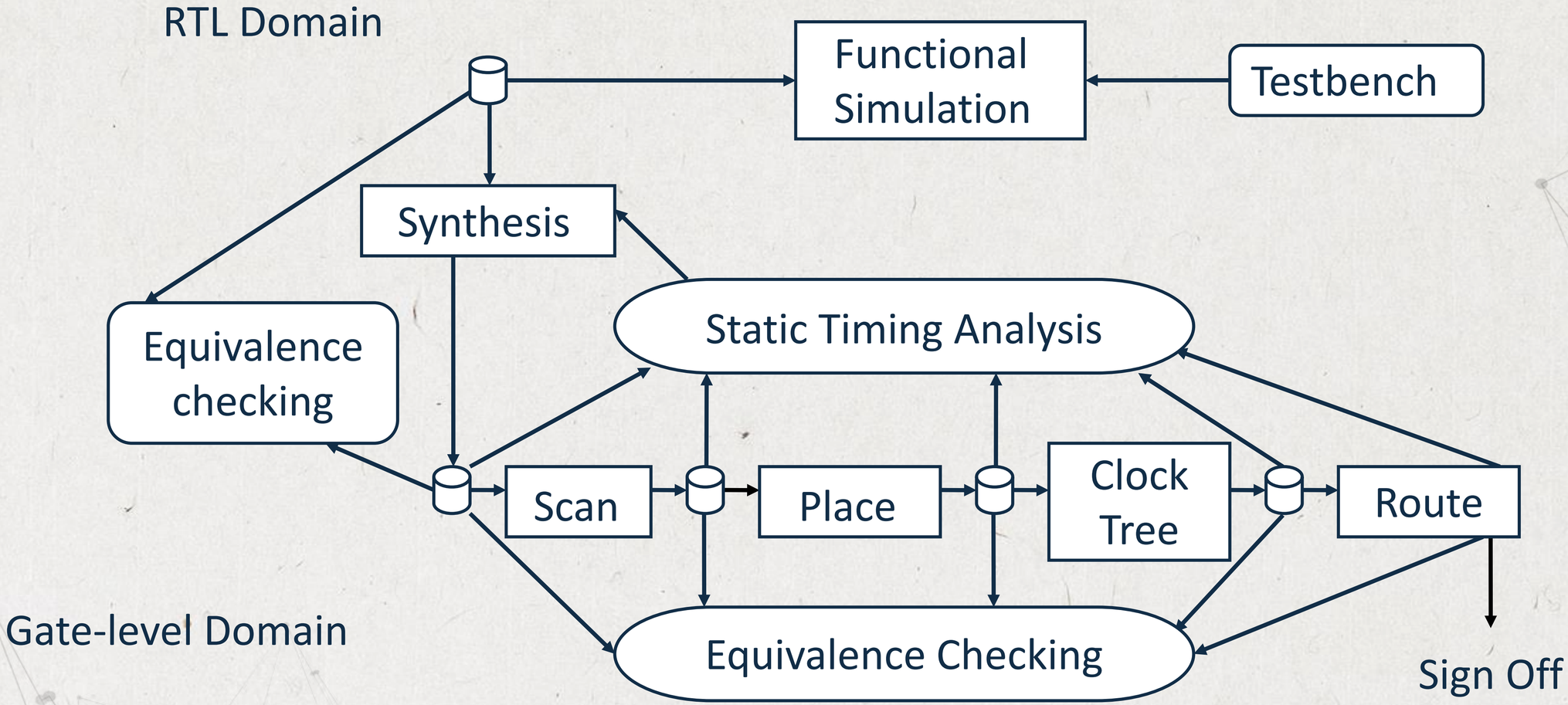
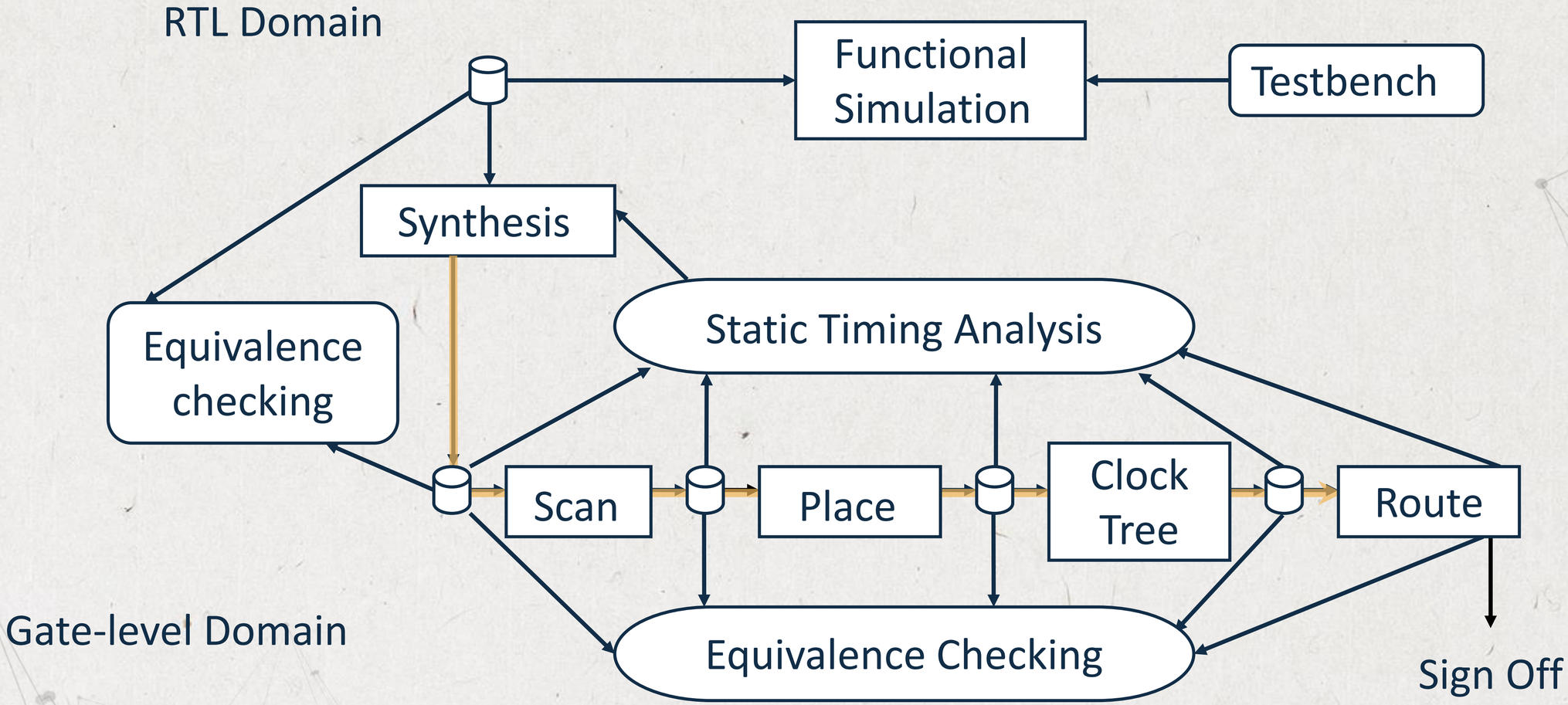
STA Flow


RTL Domain
Functional Simulation
Testbench
Synthesis
Equivalence checking
Static Timing Analysis
Scan
Place
Clock Tree
Route
Gate-level Domain
Equivalence Checking
Sign Off

STA Flow


RTL Domain
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Sign Off

STA Vs Event Simulation

	Event Driven Timing simulati	STA
Vector Generation	Required	Not Required
Design Coverage	Vector dependent(limited) coverage	Vector independent exhaustive coverage
Runtime	Takes several days/weeks of CPU time	**Analyzes multimillion gate design in hours**
Capacity	Can run out of memory for multimillion designs	**Can easily handle multimillion designs**
Analysis/Debug features	No special features for timing analysis	Features such as min/mux analysis, on chip variation, dynamic loop breaking case
Design style support	No Restrictions	Limited support for

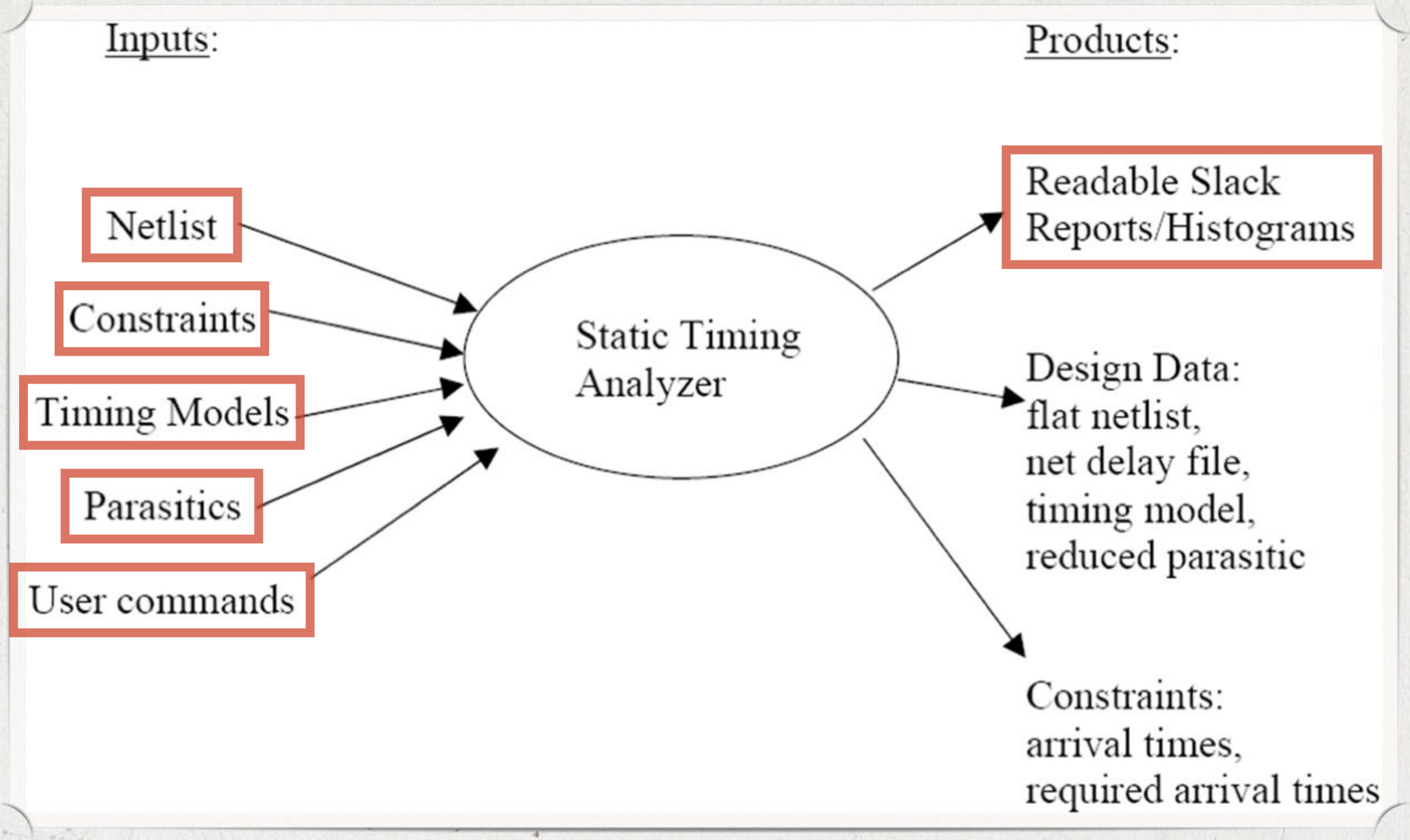
计算时间快

互补

占内存较小

只能分析同步电路，不能分析异步电路

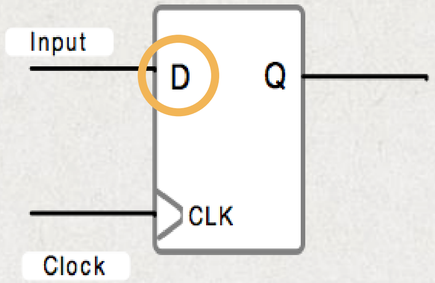
How STA Work?

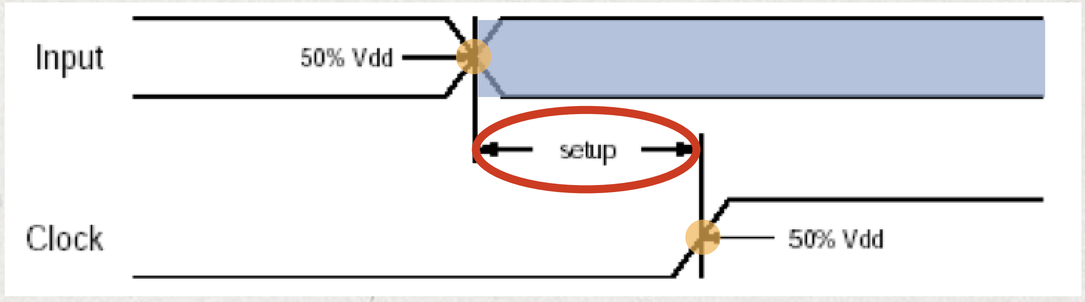

Inputs:
Products:
Netlist
Constraints
Timing Models
Parasitics
User commands
Static Timing Analyzer
Readable Slack Reports/Histograms
Design Data: flat netlist, net delay file, timing model, reduced parasitic
Constraints: arrival times, required arrival times


SYNOPSYS®
Prime Time

Setup Time

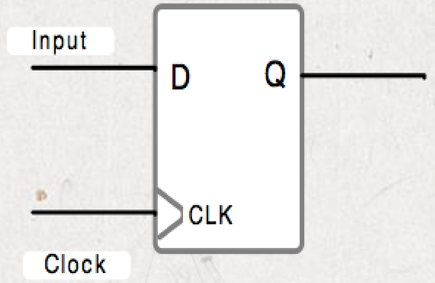
- The length of time that data must stabilize before the clock transition.

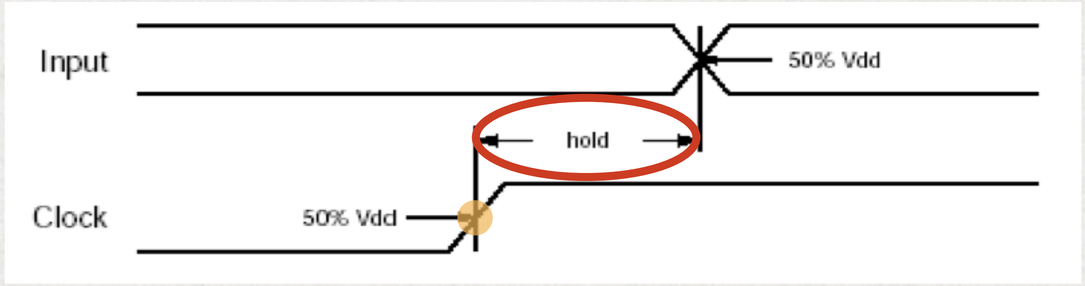




Hold Time

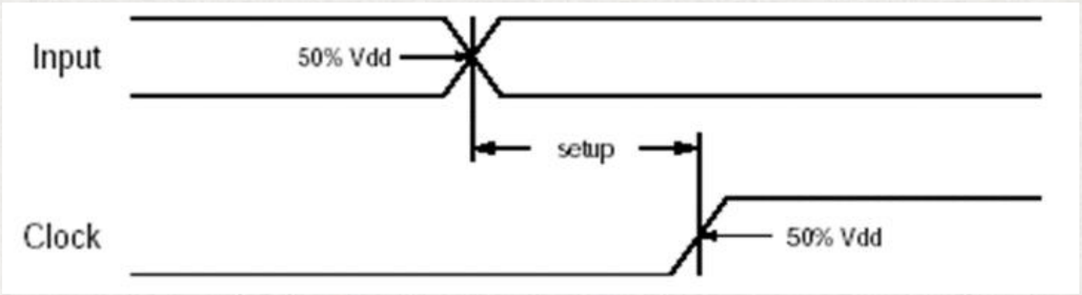
- The length of time that data must remain stable at the input pin after the active clock transition.





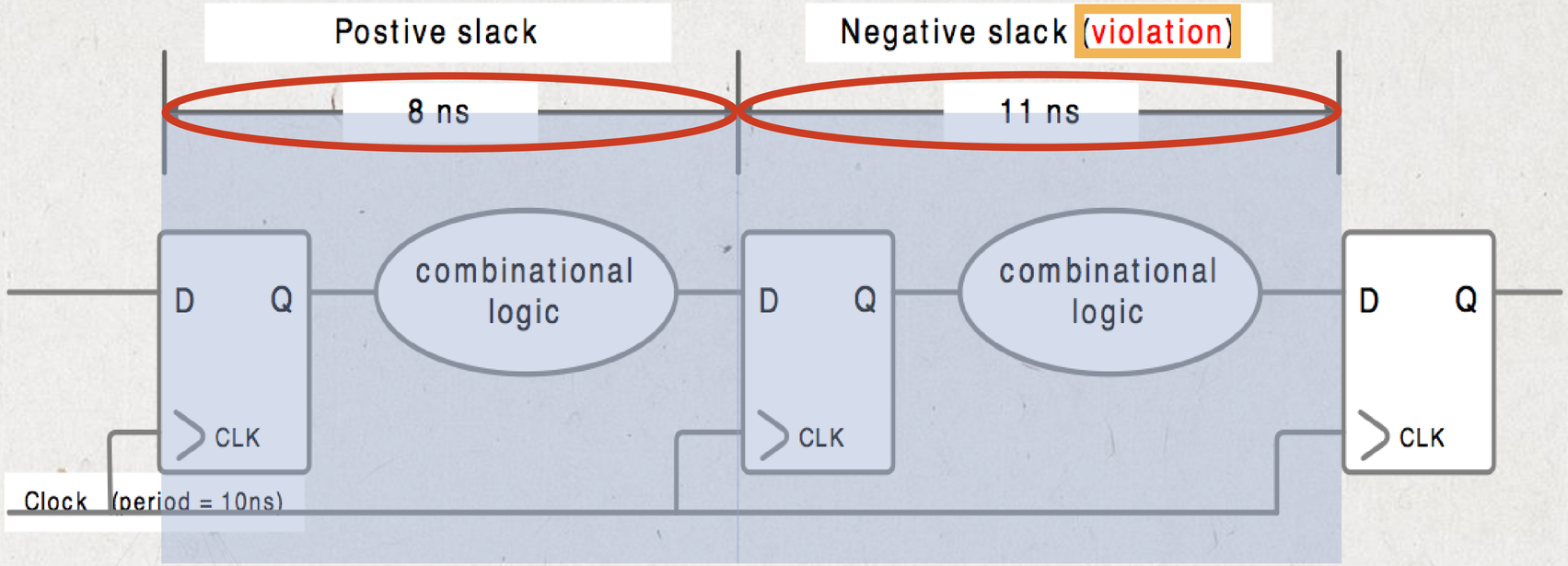
Time Slack

- Slacks is used to describe how much of the budget did the logic used up.
- Slack - the resulting margin between required & actual time of signal traveling in the path.
  - Positive slack or zero means meet constraints
  - Negative slack means violate constraint



Speed vs. Slack

- The worst case logic path determine the maximum speed (minimum clock period) for a synchronous system
- Example: clock period = 10 ns



slack=10-8=2 ≥ 0 slack=10-11=-1 < 0 clock period = 10 ns

时钟频率 → 整个电路的运行速度

翻转的次数越多

数据量计算量大

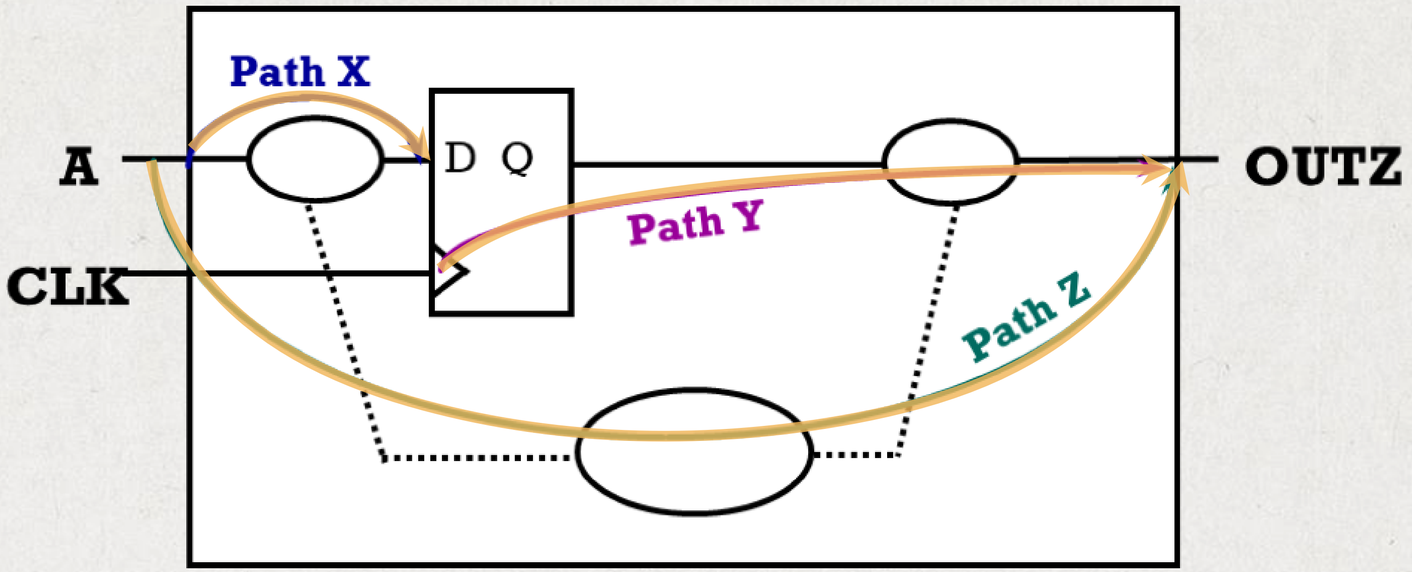
主频越高

处理器性能越高

Power vs. Slack

- Large positive slack
  - Large size
  - Large power

Three Steps in Static Timing Analysis



工艺库

STA involves three main steps:

① Design is broken down into sets of timing paths

② Delay of each path is calculated

③ Path delays are checked to see if timing constraints have been met

静态数据分析

逻辑综合

布局布线

时钟树综合

逻辑综合

时序分析

逻辑综合

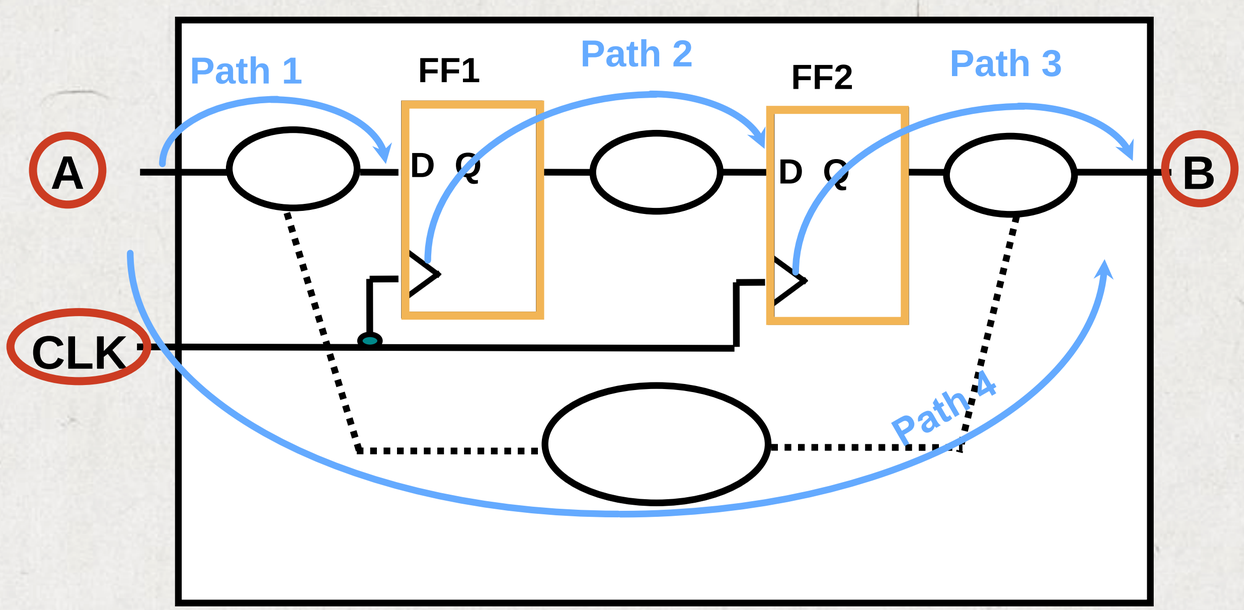
时钟网络的延迟=0

布局布线

时钟树的走线延迟、buffer分布精确

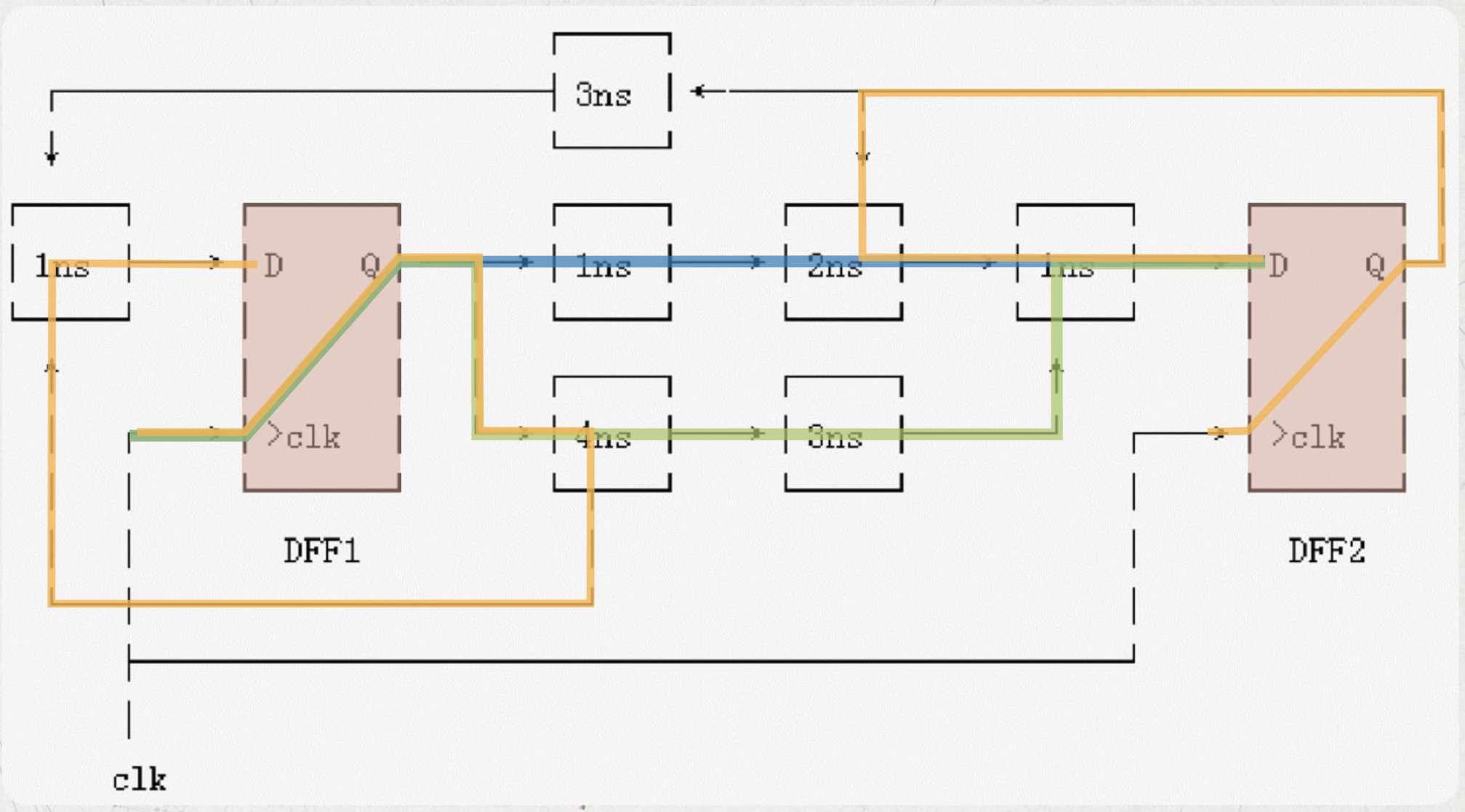
时钟网络延迟

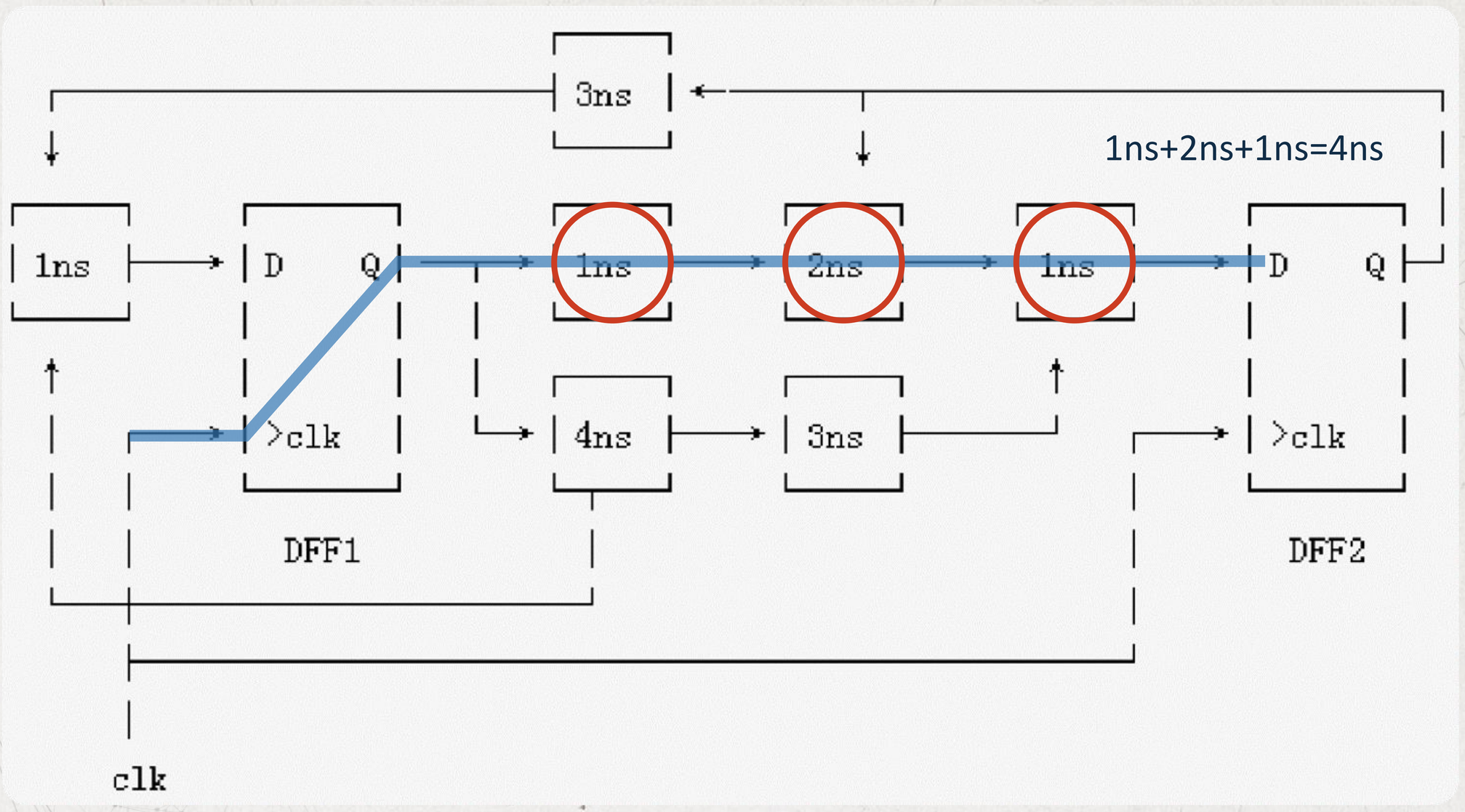
静态数据分析结果

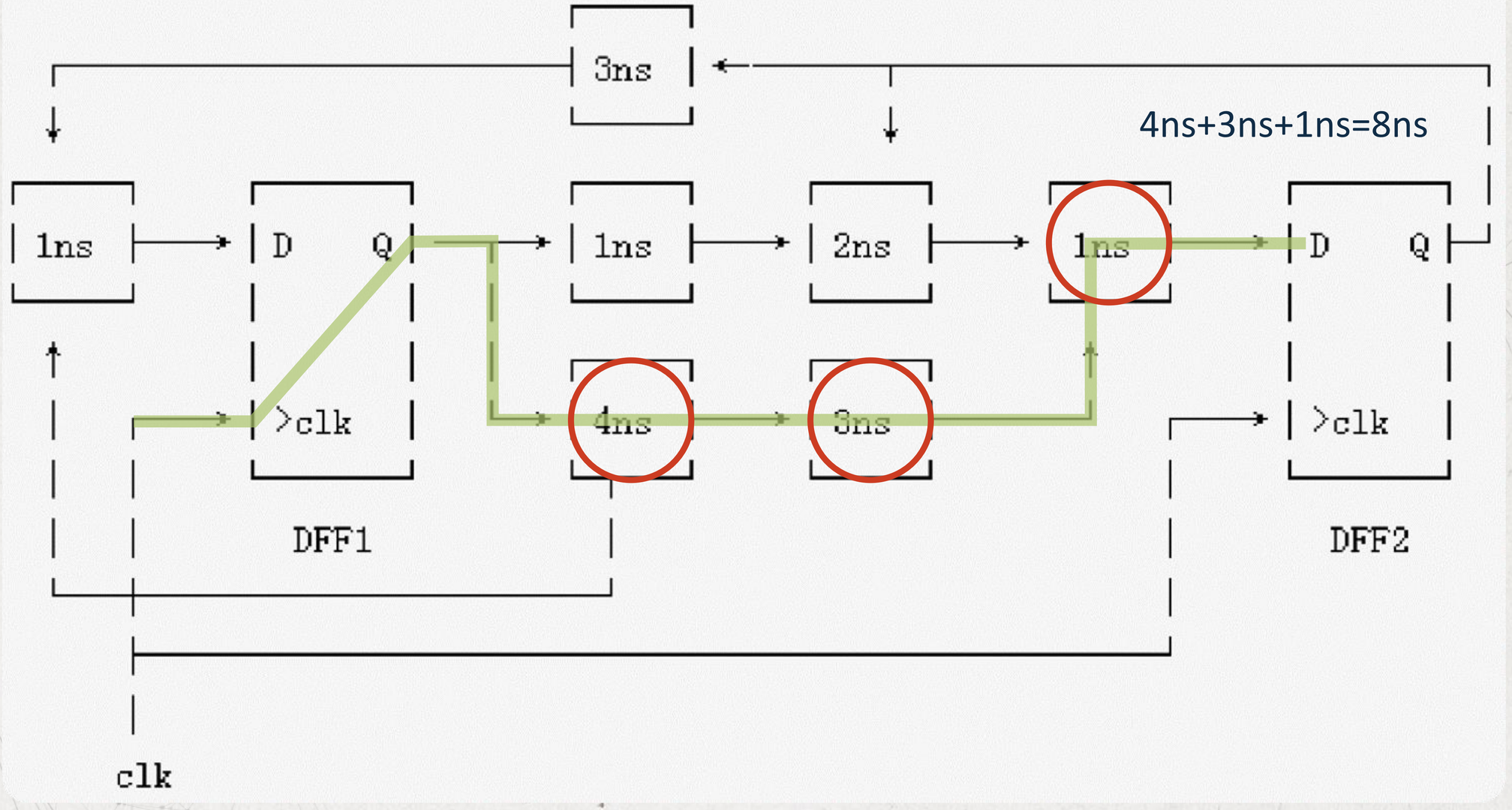


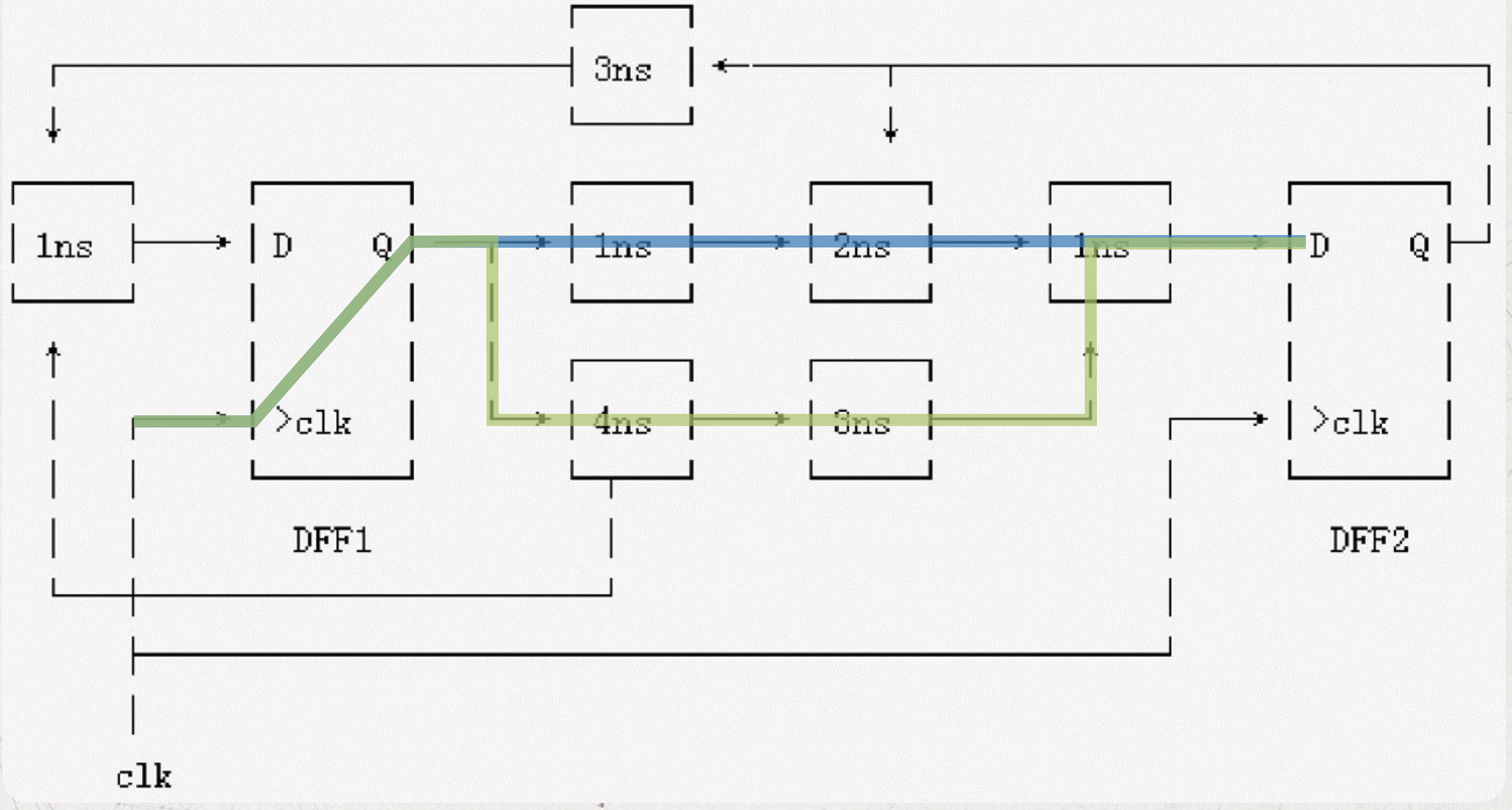
PrimeTime breaks designs into sets of paths.
There are 4 types of PrimeTime paths:

- Input port to data pin of flip-flop (Path 1)
- Clock pin of flip-flop to data pin of flip-flop (Path 2)
- Clock pin of flip-flop to output port (Path 3)
- Input port to output port (Path 4)


3ns
1ns
D
Q
1ns
2ns
1ns
D
Q
>clk
4ns
3ns
>clk
DFF1
DFF2
clk

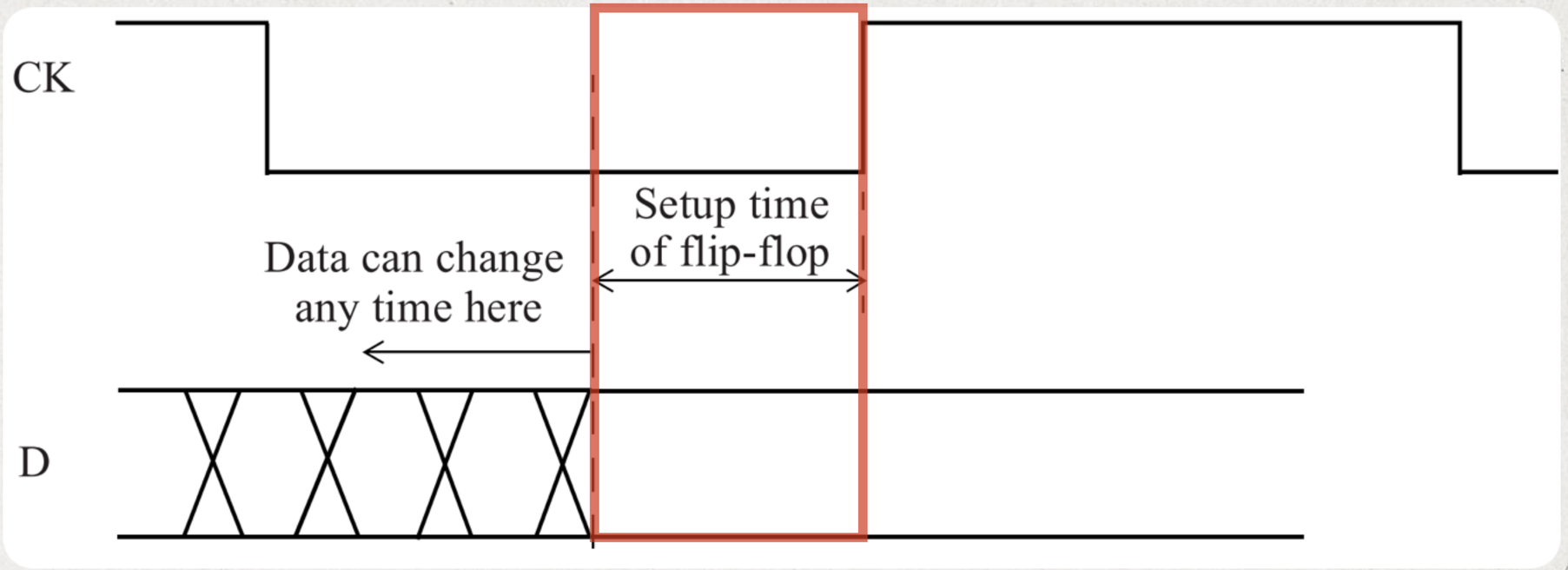

3ns
1ns+2ns+1ns=4ns
1ns
D
Q
1ns
2ns
1ns
D
Q
>clk
4ns
3ns
>clk
DFF1
DFF2
clk


3ns
4ns+3ns+1ns=8ns
1ns
D
Q
1ns
2ns
1ns
D
Q
>clk
4ns
3ns
>clk
DFF1
DFF2
clk

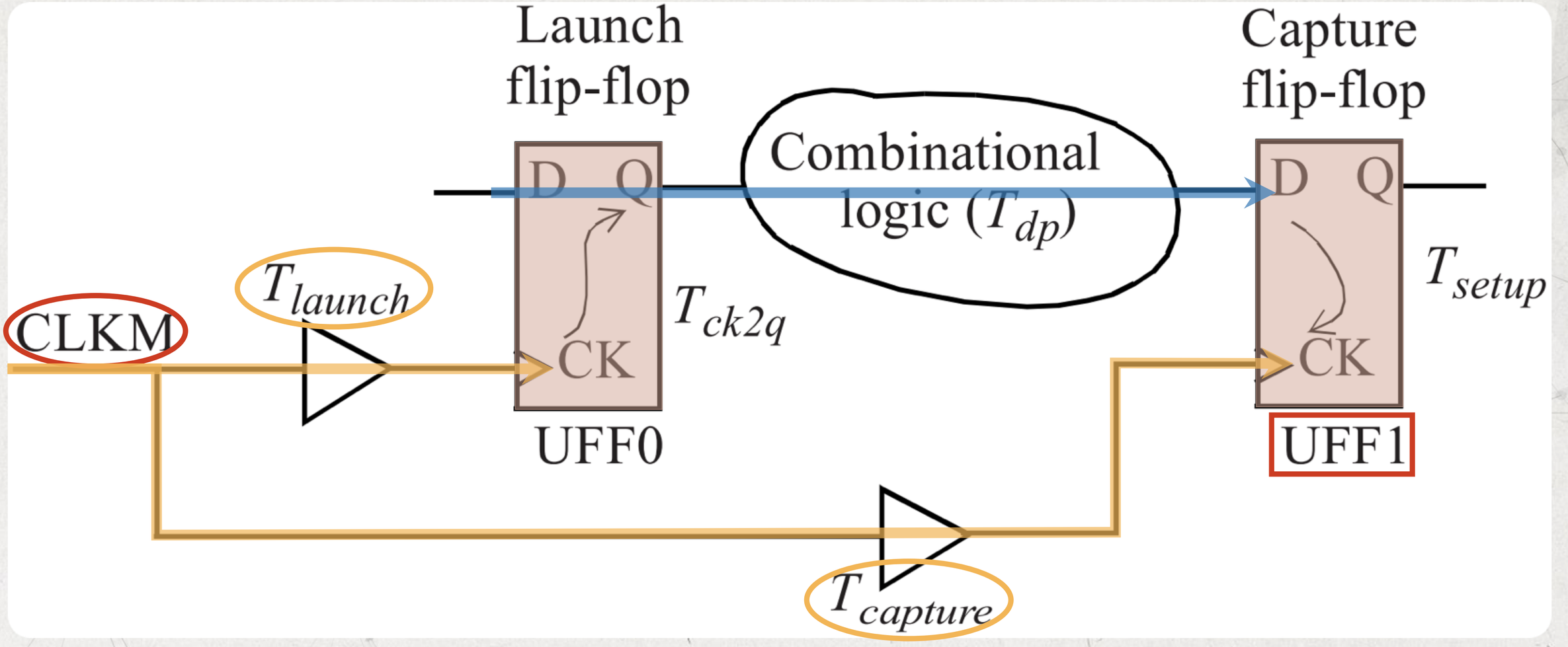

3ns
1ns
D
Q
1ns
2ns
1ns
D
Q
>clk
4ns
3ns
>clk
DFF1
DFF2
clk

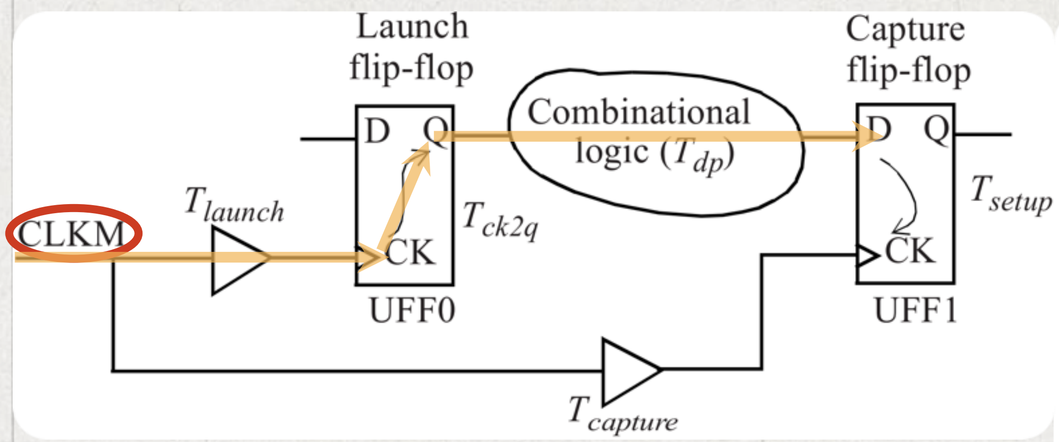
Setup timing check

A setup timing check verifies the timing relationship between the clock and the data pin of a flip-flop so that the setup requirement is met.

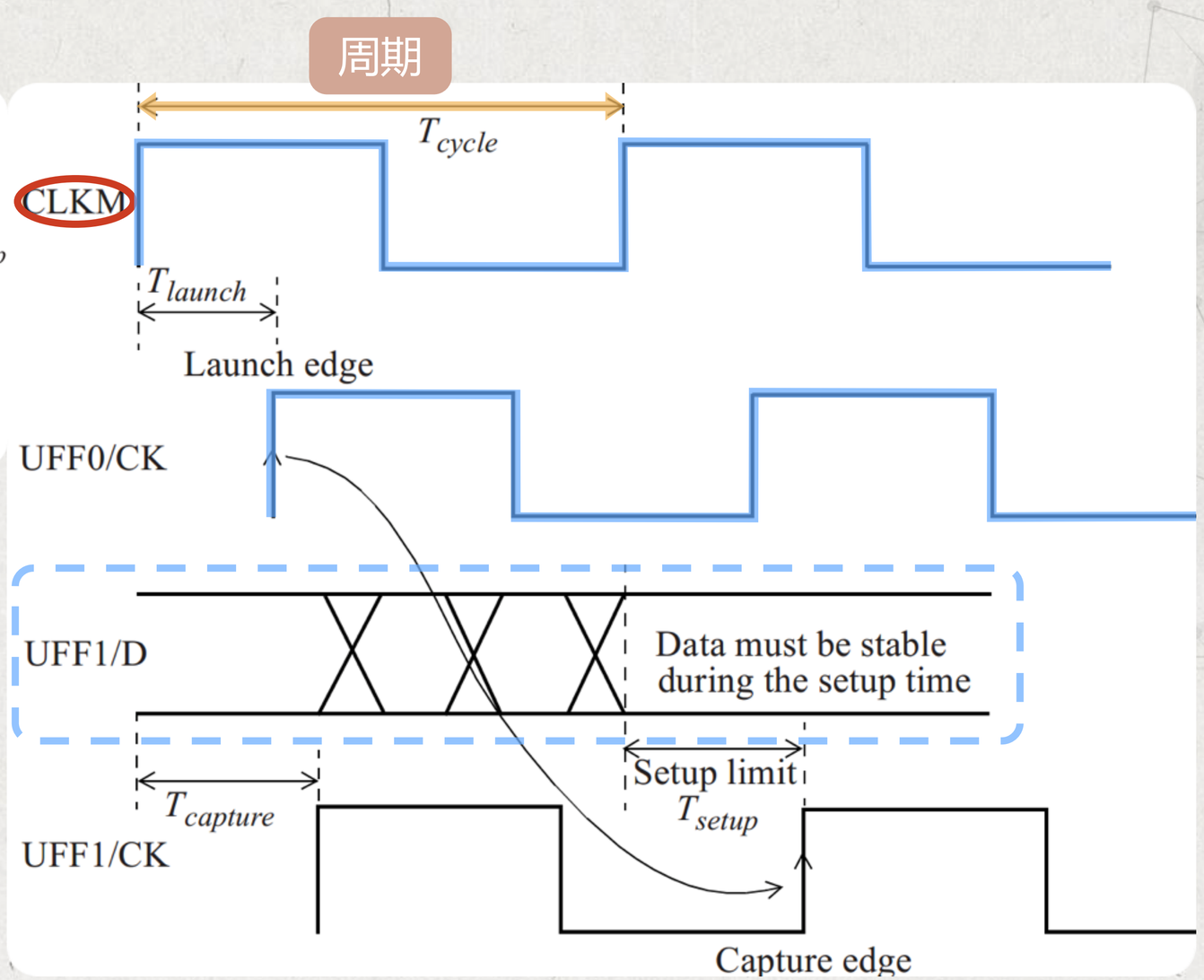


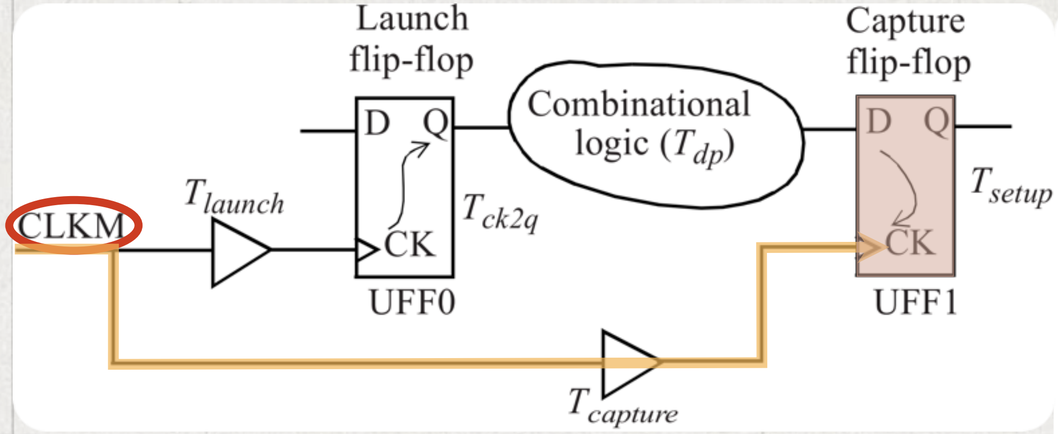
Setup requirement of a flip-flop


Launch
flip-flop
Capture
flip-flop
Combinational
logic (T_{dp})
D
Q
CK
T_{ck2q}
T_{setup}
T_{launch}
CLKM
UFF0
UFF1
$T_{capture}$



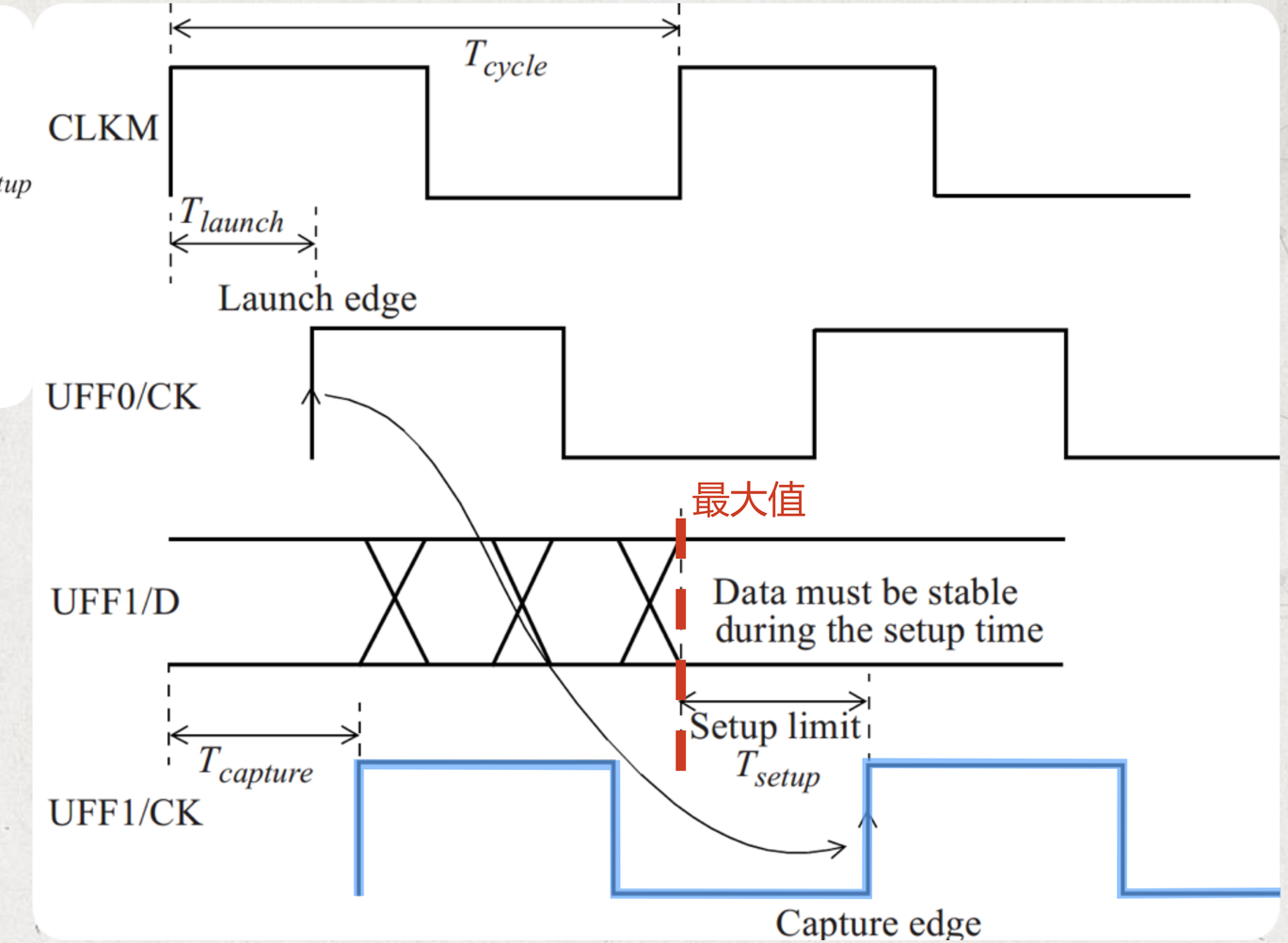
Launch路径，发射路径

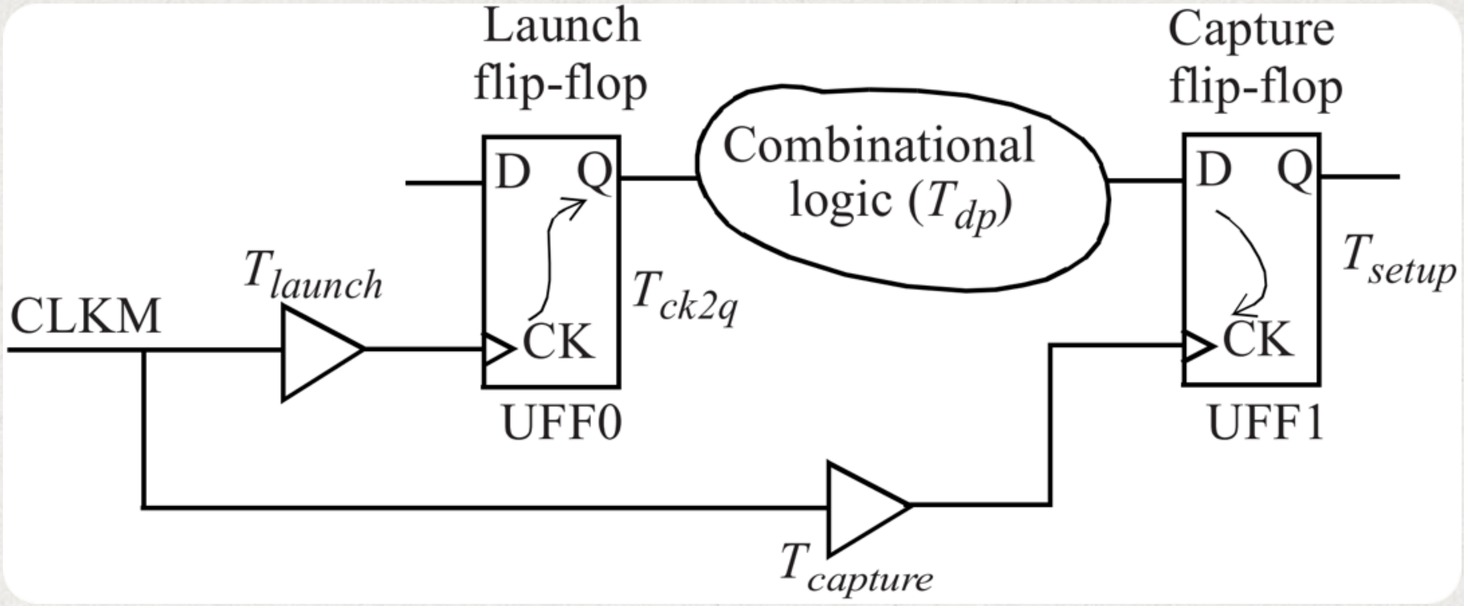



Launch
flip-flop
Capture
flip-flop
Combinational
logic (T_{dp})
D
Q
CK
CLKM
T_{launch}
T_{ck2q}
T_{setup}
$T_{capture}$
UFF0
UFF1

捕获路径


0
t


T_{cycle}
CLKM
T_{launch}
Launch edge
UFF0/CK
最大值
UFF1/D
Data must be stable
during the setup time
Setup limit
T_{setup}
$T_{capture}$
UFF1/CK
Capture edge



The setup check can be mathematically expressed as:

$$T_{launch} + T_{ck2q} + T_{dp} < T_{capture} + T_{cycle} - T_{setup}$$

- T_{launch}: the delay of the clock tree of the launch flip-flop UFF0
- T_{dp}: the delay of the combinational logic data path
- $T_{capture}$: the delay of the clock tree for the capture flip-flop UFF1
- T_{cycle}: clock period

Flip-flop to Flip-flop Path

触发器到触发器路径

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                              Incr       Path
-----------------------------------------------------------------------
clock CLKM (rise edge)                             0.00       0.00
clock network delay (ideal)                        0.00       0.00
UFF0/CK (DFF )                                     0.00       0.00 r
UFF0/Q (DFF ) <-                                   0.16       0.16 f
UNOR0/ZN (NR2  )                                   0.04       0.20 r
UBUF4/Z (BUFF  )                                   0.05       0.26 r
UFF1/D (DFF )                                      0.00       0.26 r
data arrival time                                             0.26
```

Flip-flop to Flip-flop Path

clock CLKM (rise edge)	**10.00**	10.00
clock network delay (ideal)	0.00	10.00
clock uncertainty	-0.30	9.70
UFF1/CK (DFF)		9.70 r
library setup time	-0.04	9.66
data required time		9.66
---	---	---
data required time		9.66
data arrival time		-0.26
---	---	---
slack (MET)		9.41

Question

① What are the start point and the end point of this path?

② Which Path Group is this path belong to?

③ Path Type?

④ Constrain?