芯动力——硬件加速设计方法

第五章 静态时序分析(2)

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Flip-flop to Flip-flop Path

Startpoint: UFF0 (**rising edge-triggered flip-flop clocked by CLKM**)
Endpoint: UFF1 (**rising edge-triggered flip-flop clocked by CLKM**)
Path Group: CLKM
Path Type: max

Point	Incr	Path
clock CLKM (rise edge)	**0.00**	0.00
clock network delay (ideal)	0.00	0.00
UFF0/CK (DFF)	0.00	0.00 r
UFF0/Q (DFF) <-	0.16	0.16 f
UNOR0/ZN (NR2)	0.04	0.20 r
UBUF4/Z (BUFF)	0.05	0.26 r
UFF1/D (DFF)	0.00	0.26 r
data arrival time		0.26

Flip-flop to Flip-flop Path

clock CLKM (rise edge)	**10.00**	10.00
clock network delay (ideal)	0.00	10.00
clock uncertainty	-0.30	9.70
UFF1/CK (DFF)		9.70 r
library setup time	-0.04	9.66
data required time		9.66
---	---	---
data required time		9.66
data arrival time		-0.26
---	---	---
slack (MET)		9.41

Question

① What are the start point and the end point of this path?

② Which Path Group is this path belong to?

③ Path Type?

④ Constrain?

Flip-flop to Flip-flop Path

② which Path Group is this path belong to?

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                   Incr       Path
-----------------------------------------------------------
clock CLKM (rise edge)                  0.00       0.00
clock network delay (ideal)             0.00       0.00
UFF0/CK (DFF )                          0.00       0.00 r
UFF0/Q (DFF ) <-                        0.16       0.16 f
UNOR0/ZN (NR2  )                        0.04       0.20 r
UBUF4/Z (BUFF  )                        0.05       0.26 r
UFF1/D (DFF )                           0.00       0.26 r
data arrival time                                  0.26
```

The Path Group line indicates that it belongs to the path group CLKM

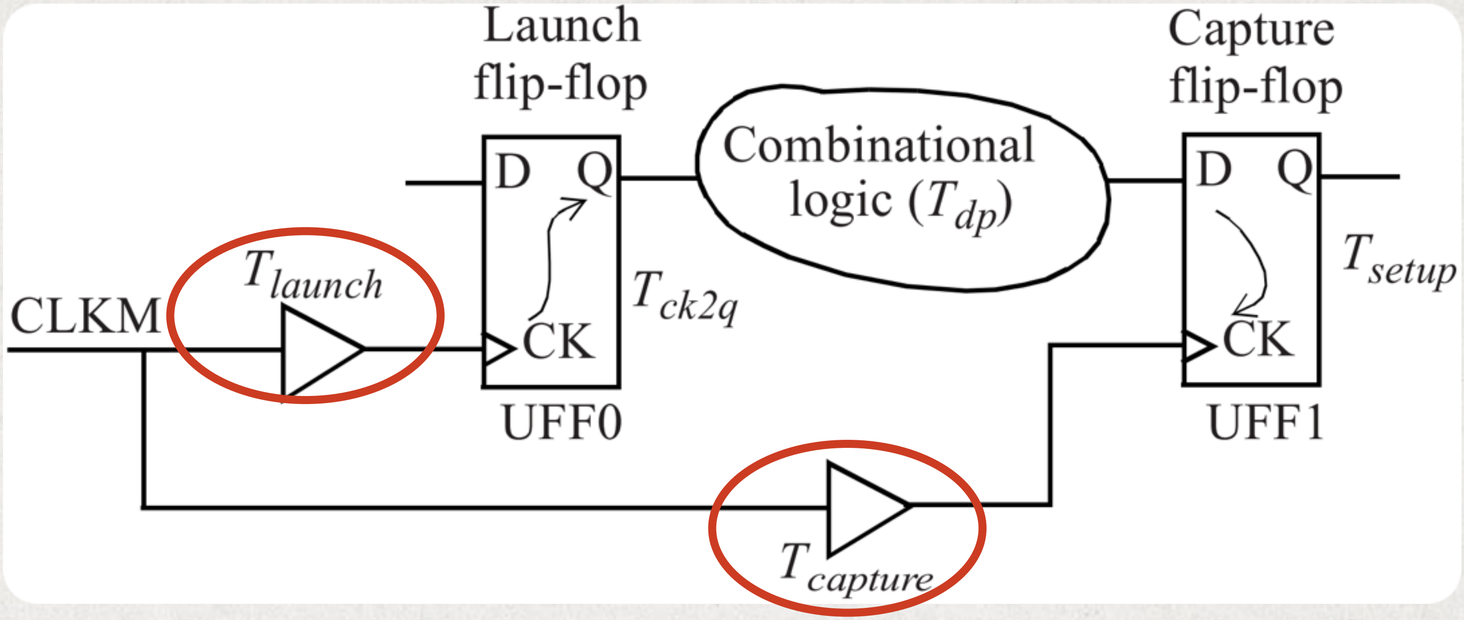
① what are the start point and the end point of this path?

Flip-flop to Flip-flop Path

③ Path Type?

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                              Incr       Path
-----------------------------------------------------------------------
clock CLKM (rise edge)                             0.00       0.00
clock network delay (ideal)                        0.00       0.00
UFF0/CK (DFF )                                     0.00       0.00 r
UFF0/Q (DFF ) <-                                   0.16       0.16 f
UNOR0/ZN (NR2  )                                   0.04       0.20 r
UBUF4/Z (BUFF  )                                   0.05       0.26 r
UFF1/D (DFF )                                      0.00       0.26 r
data arrival time                                             0.26
```



The setup check can be mathematically ex

取一个最大值

$$T_{launch} + T_{ck2q} + T_{dp} < T_{capture} + T_{cycle} - T_{setup}$$

the delay of the clock tree of the launch flip-flop UFF0

clock period

the delay of the combinational logic data path

the delay of the clock tree for the capture flip-flop UFF1

Flip-flop to Flip-flop Path

③ Path Type?

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max
```

min

```
Point                                              Incr       Path
-----------------------------------------------------------------------
clock CLKM (rise edge)                             0.00       0.00
clock network delay (ideal)                        0.00       0.00
UFF0/CK (DFF )                                     0.00       0.00 r
```

The Path Type line indicates that the delays shown in this report are all max path delays indicating that this is a setup check.

This is because setup checks correspond to the max (or longest path) delays through the logic.

Note that the hold checks correspond to the min (or shortest path) delays through the logic.

Flip-flop to Flip-flop Path

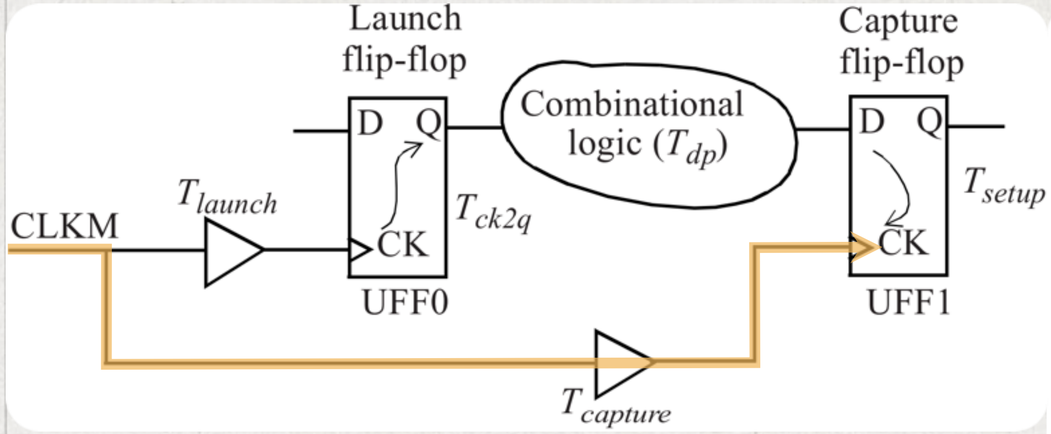
clock CLKM (rise edge)	**10.00**	10.00
clock network delay (ideal)	0.00	10.00
clock uncertainty	-0.30	9.70
UFF1/CK (DFF)		9.70 r
library setup time	-0.04	9.66
data required time		9.66
data required time		9.66
data arrival time		-0.26
slack (MET)		9.41

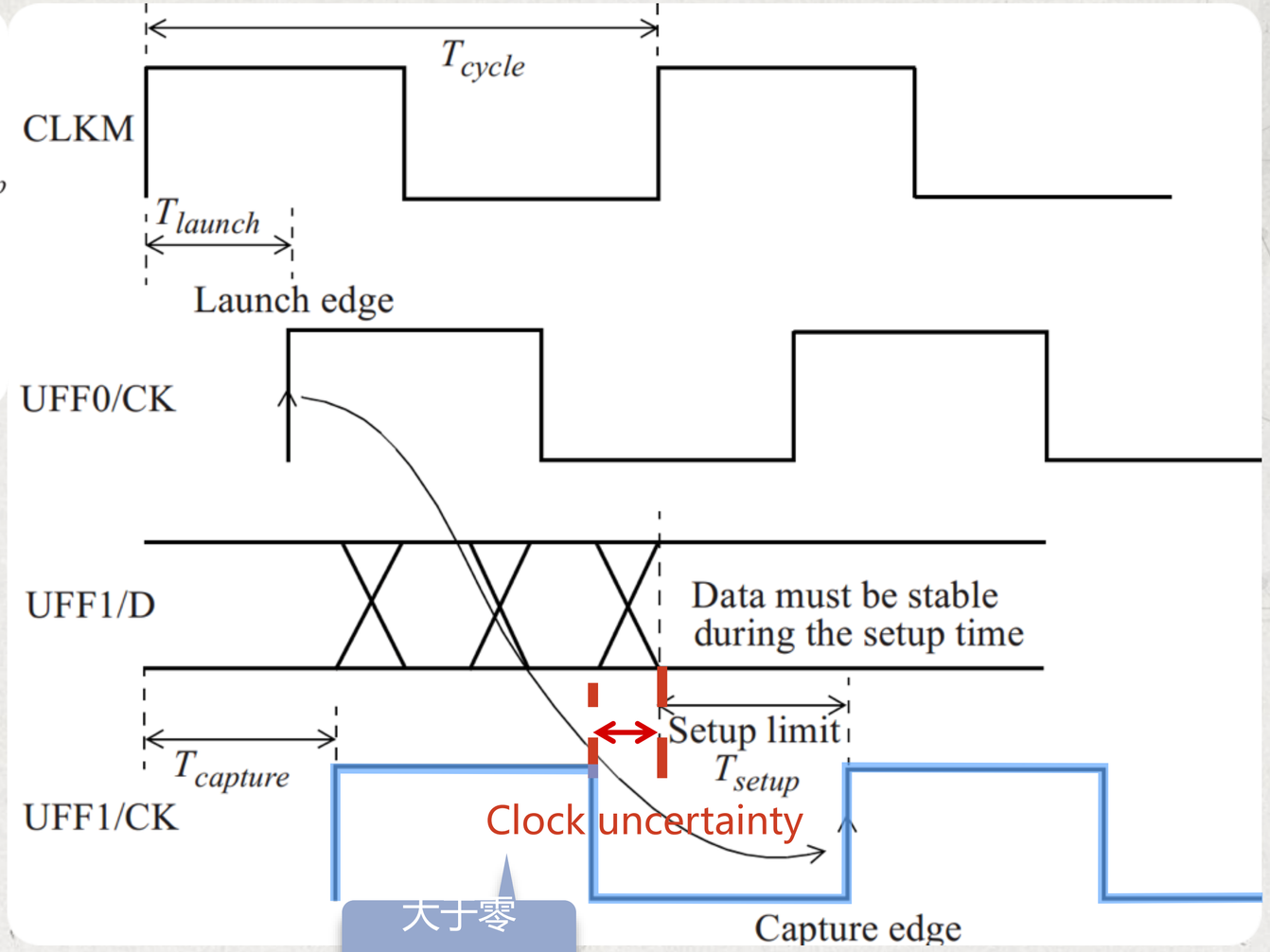
Flip-flop to Flip-flop Path

④ Constrain?

create_clock -name CLKM -period 10 -waveform {0 5} [get_ports CLKM]

```
clock CLKM (rise edge)                    10.00      10.00
clock network delay (ideal)                0.00      10.00
clock uncertainty                         -0.30       9.70
UFF1/CK (DFF )                                        9.70 r
library setup time                        -0.04       9.66
data required time                                    9.66
-----------------------------------------------------------
data required time                                    9.66
data arrival time                                    -0.26
-----------------------------------------------------------
slack (MET)                                           9.41
```


Launch
flip-flop
Capture
flip-flop
Combinational
logic (T_{dp})
D
Q
CK
CLKM
T_{launch}
T_{ck2q}
T_{setup}
$T_{capture}$
UFF0
UFF1


T_{cycle}
CLKM
T_{launch}
Launch edge
UFF0/CK
UFF1/D
Data must be stable
during the setup time
Setup limit
T_{setup}
$T_{capture}$
UFF1/CK
Clock uncertainty
大于零
Capture edge

Flip-flop to Flip-flop Path

set_ideal_network

dont_touch

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                              Incr       Path
-----------------------------------------------------------------------
clock CLKM (rise edge)                             0.00       0.00
clock network delay (ideal)                        0.00       0.00
UFF0/CK (DFF )                                     0.00       0.00 r
UFF0/Q (DFF ) <-                                   0.16       0.16 f
UNOR0/ZN (NR2  )                                   0.04       0.20 r
UBUF4/Z (BUFF  )                                   0.05       0.26 r
UFF1/D (DFF )                                      0.00       0.26 r
data arrival time                                             0.26
```

Flip-flop to Flip-flop Path

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                                   Incr       Path
-----------------------------------------------------------------------
clock CLKM (rise edge)                                  0.00       0.00
clock network delay (ideal)                             0.00       0.00
UFF0/CK (DFF )                                          0.00       0.00 r
UFF0/Q (DFF ) <-                                        0.16       0.16 f
UNOR0/ZN (NR2  )                                        0.04       0.20 r
UBUF4/Z (BUFF  )                                        0.05       0.26 r
UFF1/D (DFF )                                           0.00       0.26 r
data arrival time                                                  0.26
```

$T_{\text{launch}} = 0$

Flip-flop to Flip-flop Path

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                                   Incr       Path
-----------------------------------------------------------------------
clock CLKM (rise edge)                                  0.00       0.00
clock network delay (ideal)                             0.00       0.00
UFF0/CK (DFF )                                          0.00       0.00 r
UFF0/Q (DFF ) <-                                        0.16       0.16 f
UNOR0/ZN (NR2  )                                        0.04       0.20 r
UBUF4/Z (BUFF  )                                        0.05       0.26 r
UFF1/D (DFF )                                           0.00       0.26 r
data arrival time                                                  0.26
```

$T_{ck2q}=0.16$

Flip-flop to Flip-flop Path

```
clock CLKM (rise edge)                    10.00      10.00
clock network delay (ideal)                0.00      10.00
clock uncertainty                         -0.30       9.70
UFF1/CK (DFF )                                        9.70 r
library setup time                        -0.04       9.66
data required time                                    9.66
-------------------------------------------------------------

data required time                                    9.66
data arrival time                                    -0.26
-------------------------------------------------------------

slack (MET)                                           9.41
```

Flip-flop to Flip-flop Path

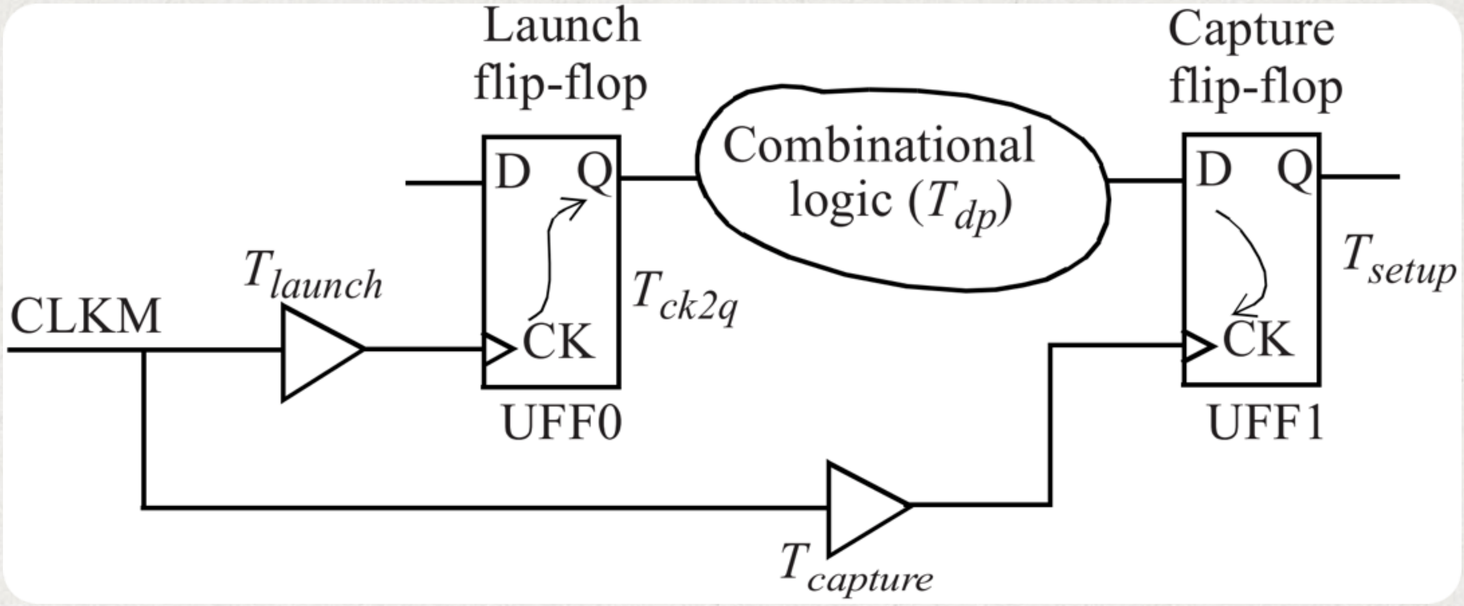
clock CLKM (rise edge)		**10.00**	10.00
clock network delay (ideal)		0.00	10.00
clock uncertainty		-0.30	9.70
UFF1/CK (DFF)			9.70 r
library setup time	$T_{\text{setup}}=0.04$	-0.04	9.66
data required time			9.66
data required time			9.66
data arrival time			-0.26
slack (MET)			9.41

Flip-flop to Flip-flop Path

clock CLKM (rise edge)	**10.00**	10.00	
clock network delay (ideal)	0.00	10.00	
clock uncertainty	-0.30	9.70	
UFF1/CK (DFF)		9.70	r
library setup time	-0.04	9.66	
data required time		9.66	
data required time		9.66	
data arrival time		-0.26	
slack (MET)		9.41	

Flip-flop to Flip-flop Path

clock CLKM (rise edge)	**10.00**	10.00
clock network delay (ideal)	0.00	10.00
clock uncertainty	-0.30	9.70
UFF1/CK (DFF)		9.70 r
library setup time	-0.04	9.66
data required time		9.66
---	---	---
data required time		9.66
data arrival time		-0.26
---	---	---
slack (MET)		9.41



$$T_{launch} + T_{ck2q} + T_{dp} < T_{capture} + T_{cycle} - T_{setup}$$

$$slack = (T_{capture} + T_{cycle} - T_{setup} - T_{uncertainty}) - (T_{launch} + T_{ck2q} + T_{dp})$$

$$\frac{0 + 10 - 0.04 - 0.30}{\text{Data required time}} - \frac{0 + 0.16 + 0.09}{\text{Data arrival time}} > 0$$

Flip-flop to Flip-flop Path

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CLKM (rise edge)                   0.00       0.00
clock network delay (ideal)              0.00       0.00
UFF0/CK (DFF )                           0.00       0.00 r
UFF0/Q (DFF ) <-                         0.16       0.16 f
UNOR0/ZN (NR2  )                         0.04       0.20 r
UBUF4/Z (BUFF  )                         0.05       0.26 r
UFF1/D (DFF )                            0.00       0.26 r
data arrival time                                   0.26
```

Flip-flop to Flip-flop Path

clock CLKM (rise edge)	**10.00**	10.00
clock network delay (ideal)	0.00	10.00
clock uncertainty	-0.30	9.70
UFF1/CK (DFF)		9.70 r
library setup time	-0.04	9.66
data required time		9.66
data required time		9.66
data arrival time		-0.26
slack (MET)		9.41

时钟网络有一个确定值的延迟值

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                              Incr       Path
-----------------------------------------------------------------------
clock CLKM (rise edge)                             0.00       0.00
clock network delay (propagated)                   0.11       0.11
UFF0/CK (DFF )                                     0.00       0.11 r
UFF0/Q (DFF ) <-                                   0.14       0.26 f
UNOR0/ZN (NR2  )                                   0.04       0.30 r
UBUF4/Z (BUFF  )                                   0.05       0.35 r
UFF1/D (DFF )                                      0.00       0.35 r
data arrival time                                             0.35
```

clock CLKM (rise edge)	10.00	10.00	
clock network delay (propagated)	**0.12**	10.12	
clock uncertainty	-0.30	9.82	
UFF1/CK (DFF)		9.82	r
library setup time	-0.04	9.78	
data required time		9.78	
data required time		9.78	
data arrival time		-0.35	
slack (MET)		9.43	

0.12-0.11=0.01

时钟的偏斜

- The timing path report can optionally include the expanded clock paths, that is, with the clock trees explicitly shown. Here is such an example.

Point	Incr	Path	
clock CLKM (rise edge)	0.00	0.00	
clock source latency	0.00	0.00	
CLKM (in)	**0.00**	**0.00**	**r**
UCKBUF0/C (CKB)	**0.06**	**0.06**	**r**
UCKBUF1/C (CKB)	**0.06**	**0.11**	**r**
UFF0/CK (DFF)	0.00	0.11	r
UFF0/Q (DFF) <-	0.14	0.26	**f**
UNOR0/ZN (NR2)	0.04	0.30	r
UBUF4/Z (BUFF)	0.05	0.35	r
UFF1/D (DFF)	0.00	0.35	**r**
data arrival time		0.35	

clock CLKM (rise edge)	10.00	10.00	
clock source latency	0.00	10.00	
CLKM (in)	**0.00**	**10.00**	**r**
UCKBUF0/C (CKB)	**0.06**	**10.06**	**r**
UCKBUF2/C (CKB)	**0.07**	**10.12**	**r**
UFF1/CK (DFF)	0.00	10.12	r
clock uncertainty	-0.30	9.82	
library setup time	-0.04	9.78	
data required time		9.78	
data required time		9.78	
data arrival time		-0.35	
slack (MET)		9.43	

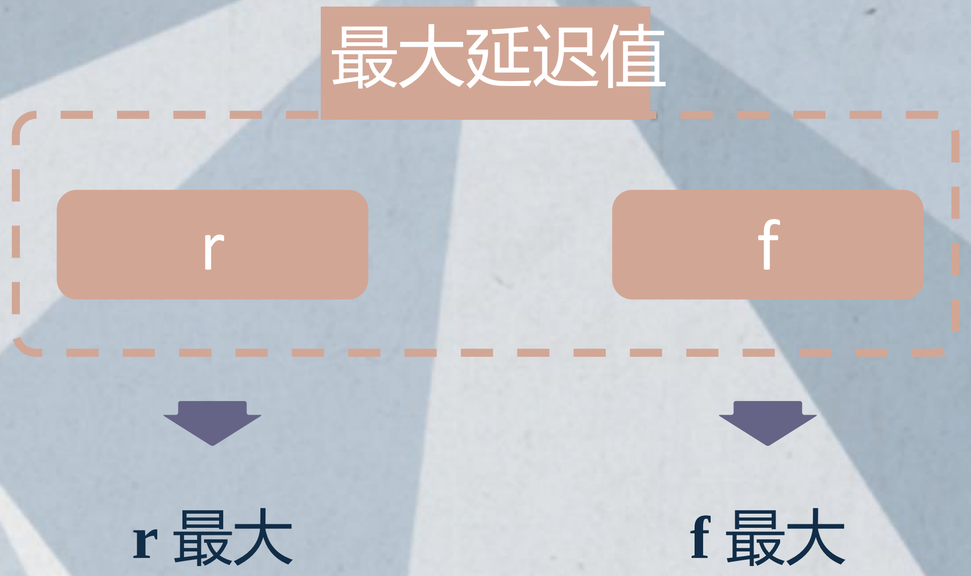
- The “r” and “f” characters in the timing report indicate the rising (and falling) edge of the clock or data signal. The previous path report shows the path starting from the falling edge of UFF0/Q and ending on the rising edge of UFF1/D. Since UFF1/D can be either 0 or 1, there can be a path ending at the falling edge of UFF1/D as well. Here is such a path.

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CLKM (rise edge)                   0.00       0.00
clock source latency                     0.00       0.00
CLKM (in)                                0.00       0.00 r
UCKBUF0/C (CKB  )                        0.06       0.06 r
UCKBUF1/C (CKB  )                        0.06       0.11 r
UFF0/CK (DFF )                           0.00       0.11 r
UFF0/Q (DFF ) <-                         0.14       0.26 r
UNOR0/ZN (NR2  )                         0.02       0.28 f
UBUF4/Z (BUFF  )                         0.06       0.33 f
UFF1/D (DFF )                            0.00       0.33 f
data arrival time                                   0.33
```

从逻辑零翻转到逻辑1产生的延迟

从逻辑1翻转到逻辑0产生的延迟

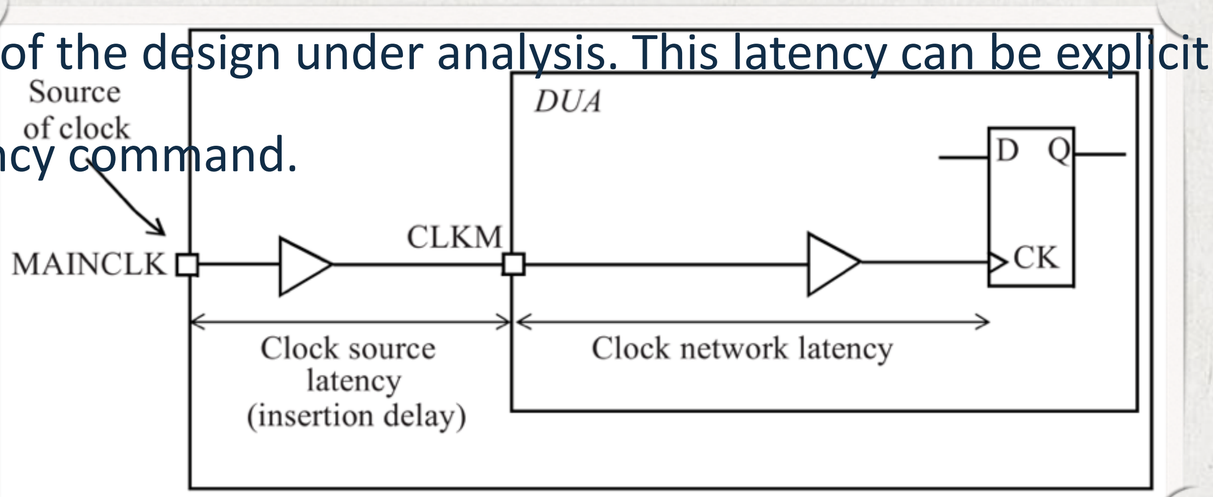

最大延迟值
r
f
r 最大
f 最大

- Note that the edge at the clock pin of the flip-flop (called the active edge) remains unchanged. It can only be a rising or falling active edge, depending upon whether the flip-flop

```
clock CLKM (rise edge)                    10.00       10.00
clock source latency                       0.00       10.00
CLKM (in)                                  0.00       10.00 r
UCKBUF0/C (CKB  )                          0.06       10.06 r
UCKBUF2/C (CKB  )                          0.07       10.12 r
UFF1/CK (DFF )                             0.00       10.12 r
clock uncertainty                         -0.30        9.82
library setup time                        -0.03        9.79
data required time                                     9.79
-------------------------------------------------------------
data required time                                     9.79
data arrival time                                     -0.33
-------------------------------------------------------------
slack (MET)                                            9.46
```

What is clock source latency?

- This is also called insertion delay and is the time it takes for a clock to propagate from its source to the clock definition point of the design under analysis as depicted in Figure. This corresponds to the latency of the clock tree that is outside of the design. For example, if this design were part of a larger block, the clock source latency specifies the delay of the clock tree up to the clock pin of the design under analysis. This latency can be explicitly specified using the set_clock_latency command.



clock_latency

```
set_clock_latency -source -rise 0.7 [get_clocks CLKM]
```

```
set_clock_latency -source -fall 0.65 [get_clocks CLKM]
```