芯动力——硬件加速设计方法

第五章 静态时序分析(3)

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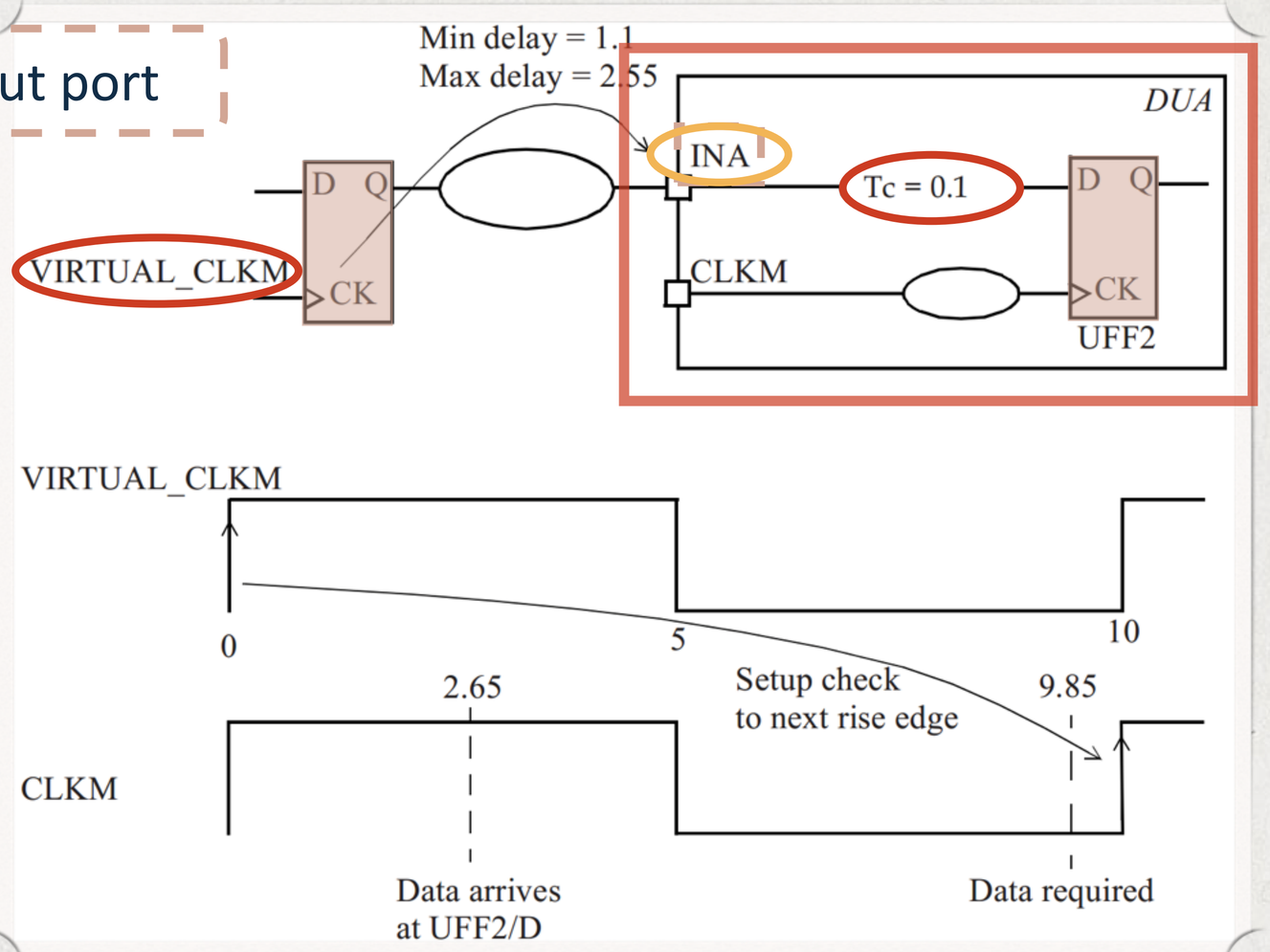
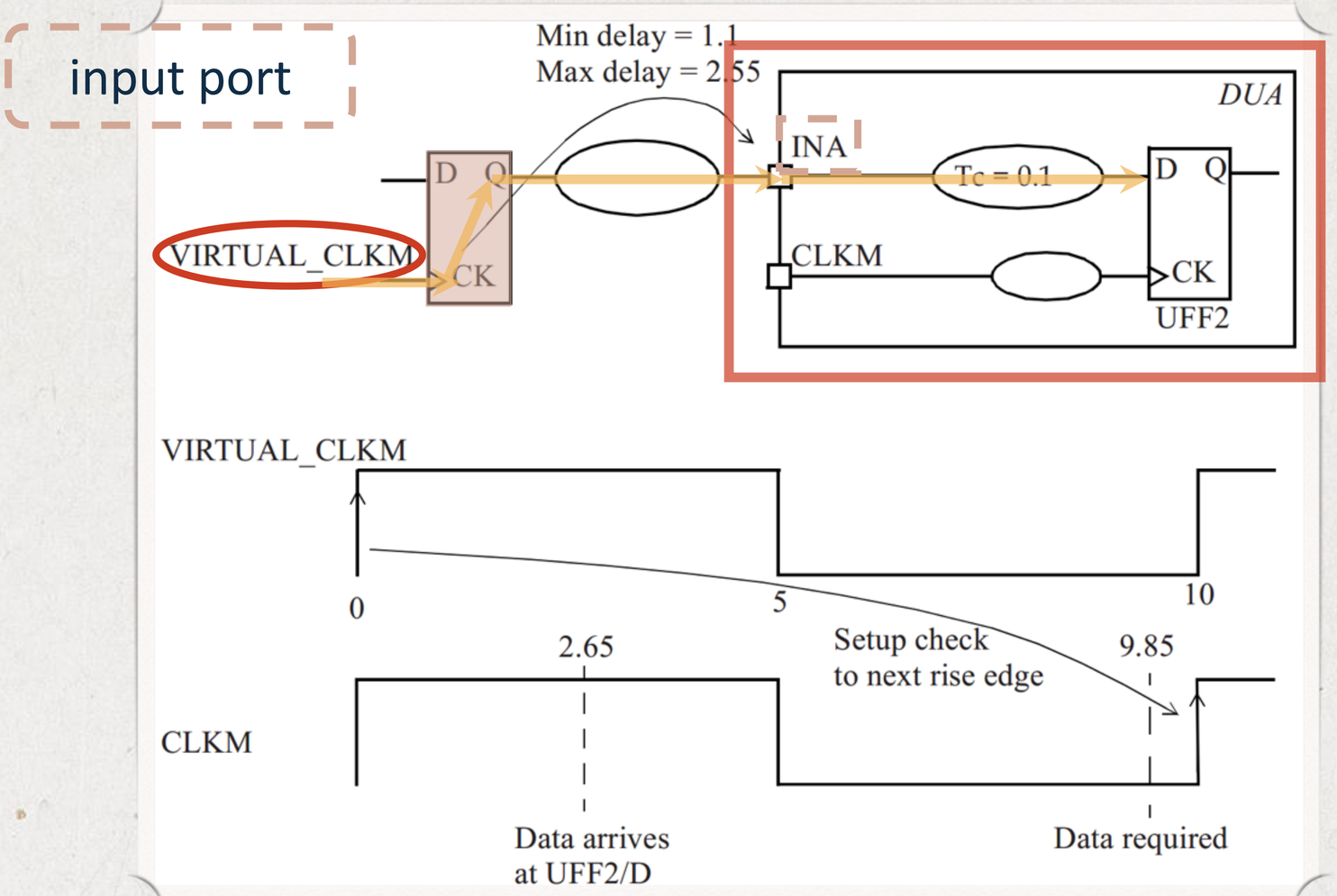
Input to Flip-flop Path

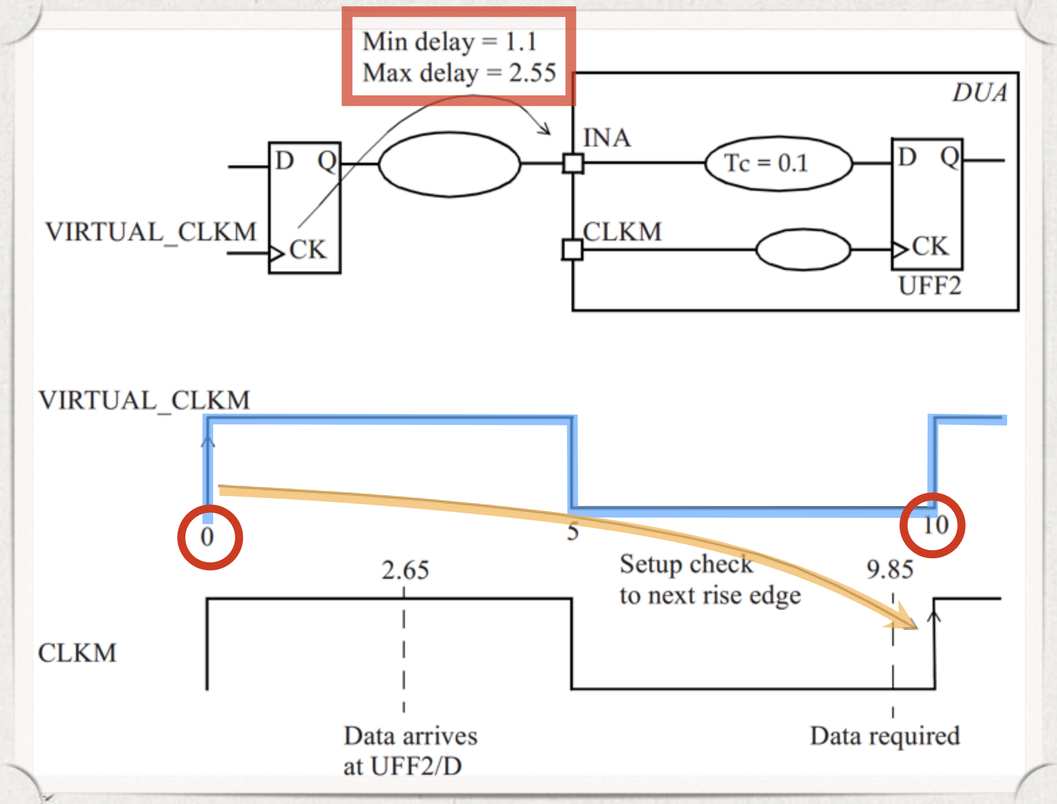
input port



Input to Flip-flop Path



Input to Flip-flop Path



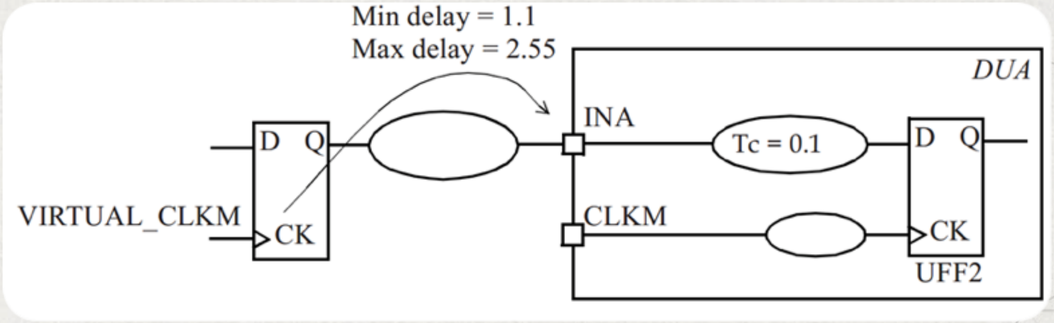
input port

- Constrain：

  creat_clock –name VIRTUAL_CLKM –period 10 –waveform {0 5}

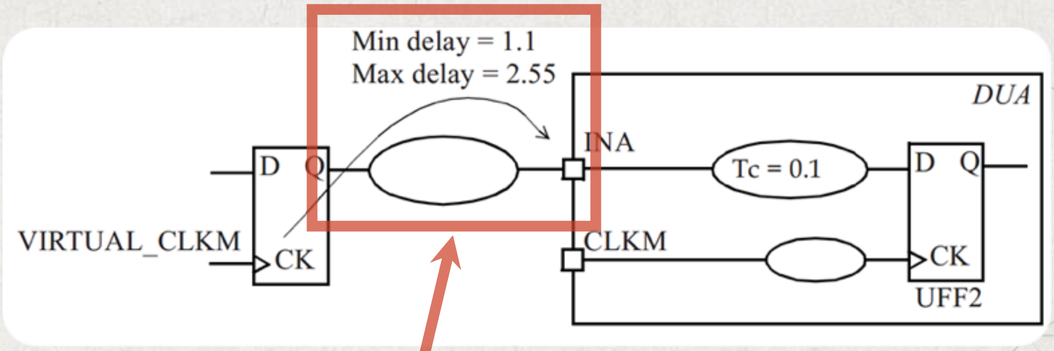
  set_input_delay –clock VIRTUAL_CLKM –max 2.55 [get_ports INA]

Input to Flip-flop Path



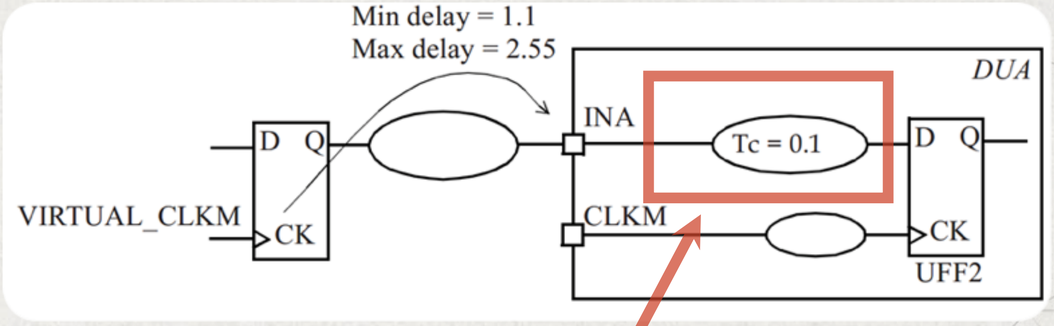

```
Startpoint: INA (input port clocked by VIRTUAL_CLKM)
Endpoint: UFF2 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                              Incr       Path
-----------------------------------------------------------------------
clock VIRTUAL_CLKM (rise edge)                     0.00       0.00
clock network delay (ideal)                        0.00       0.00
input external delay                               2.55       2.55 f
-----------------------------------------------------------------------
INA (in) <-                                        0.00       2.55 f
UINV1/ZN (INV  )                                   0.02       2.58 r
UAND0/Z (AN2  )                                    0.06       2.63 r
UINV2/ZN (INV  )                                   0.02       2.65 f
UFF2/D (DFF )                                      0.00       2.65 f
data arrival time                                             2.65
```

Input to Flip-flop Path



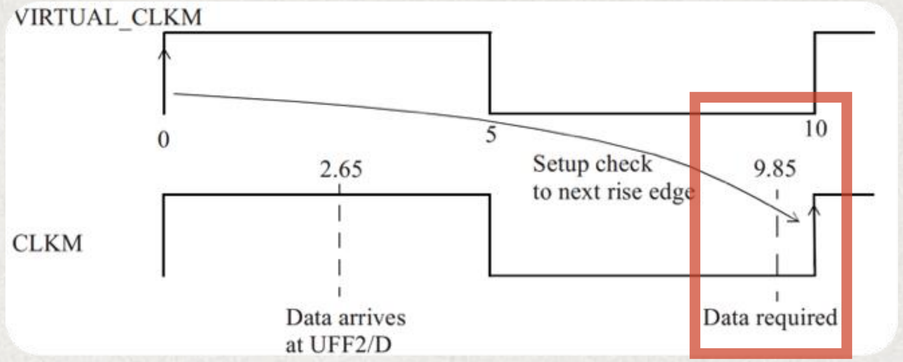

```
Startpoint: INA (input port clocked by VIRTUAL_CLKM)
Endpoint: UFF2 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                              Incr       Path
-----------------------------------------------------------------------
clock VIRTUAL_CLKM (rise edge)                     0.00       0.00
clock network delay (ideal)                        0.00       0.00
input external delay                               2.55       2.55 f
INA (in) <-                                        0.00       2.55 f
UINV1/ZN (INV  )                                   0.02       2.58 r
UAND0/Z (AN2  )                                    0.06       2.63 r
UINV2/ZN (INV  )                                   0.02       2.65 f
UFF2/D (DFF )                                      0.00       2.65 f
data arrival time                                             2.65
```

Input to Flip-flop Path

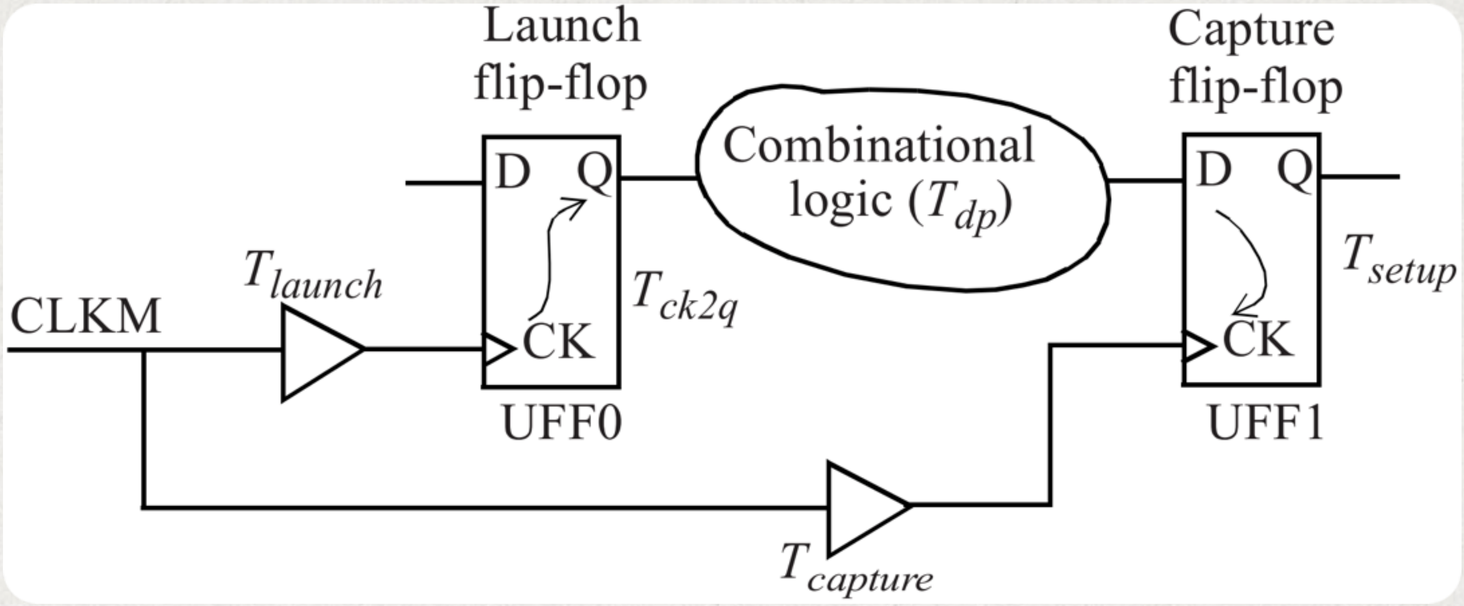



```
Startpoint: INA (input port clocked by VIRTUAL_CLKM)
Endpoint: UFF2 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: max

Point                                              Incr       Path
-----------------------------------------------------------------------
clock VIRTUAL_CLKM (rise edge)                     0.00       0.00
clock network delay (ideal)                        0.00       0.00
input external delay                               2.55       2.55 f

INA (in) <-                                        0.00       2.55 f
UINV1/ZN (INV  )                                   0.02       2.58 r
UAND0/Z (AN2  )                                    0.06       2.63 r
UINV2/ZN (INV  )                                   0.02       2.65 f
UFF2/D (DFF )                                      0.00       2.65 f
data arrival time                                             2.65
```

Input to Flip-flop Path




```
clock CLKM (rise edge)                  10.00       10.00
clock source latency                     0.00       10.00
CLKM (in)                                0.00       10.00 r
UCKBUF0/C (CKB  )                        0.06       10.06 r
UCKBUF2/C (CKB  )                        0.07       10.12 r
UCKBUF3/C (CKB  )                        0.06       10.18 r
UFF2/CK (DFF )                           0.00       10.18 r
clock uncertainty                       -0.30        9.88
library setup time                      -0.03        9.85
data required time                                   9.85
-------------------------------------------------------------
data required time                                   9.85
data arrival time                                   -2.65
-------------------------------------------------------------
slack (MET)                                          7.20
```



$$T_{\text{launch}} + T_{\text{ck2q}} + T_{\text{dp}} < T_{\text{capture}} + T_{\text{cycle}} - T_{\text{setup}}$$

$$\text{slack} = (T_{\text{capture}} + T_{\text{cycle}} - T_{\text{setup}} - T_{\text{uncertainty}}) - (T_{\text{launch}} + T_{\text{ck2q}} + T_{\text{dp}})$$

$$\frac{0 + 10 - 0.03 - 0.30}{\text{Data required time}} - \frac{0 + 2.55 + 0.1}{\text{Data arrival time}} > 0$$

Flip-flop to Output Path

- Similar to the input port constraint described above, an output port can be constrained either with respect to a virtual clock, or an internal clock of the design, or an input clock port, or an output clock port.
- To determine the delay of the last cell connected to the output port correctly, one needs to specify the load on this port. The output load is specified above using the set_load command.

```
set_output_delay -clock VIRTUAL_CLKP -max 5.1 [get_ports ROUT]
```

```
set_load 0.02 [get_ports ROUT]
```

cell的延迟

input transition

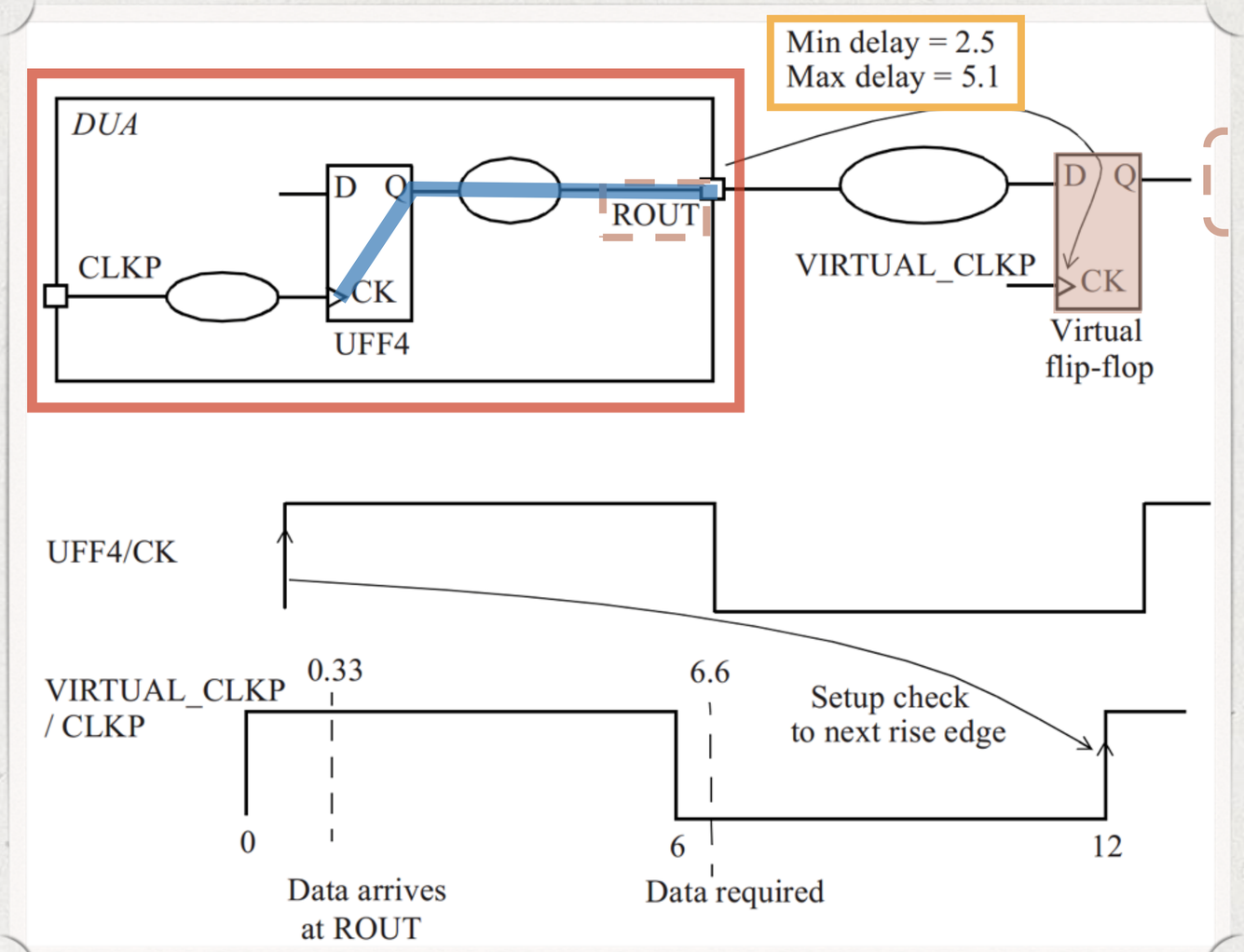
output cap

输出端口

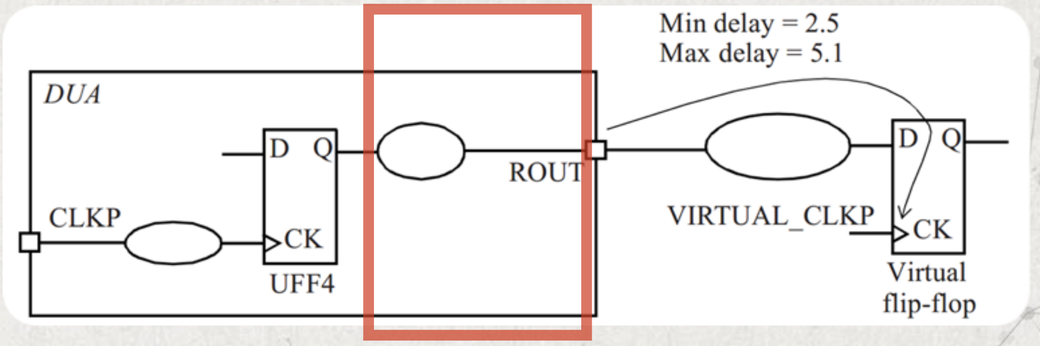
指定一个load值

标准单元的延迟值

Flip-flop to Output Path

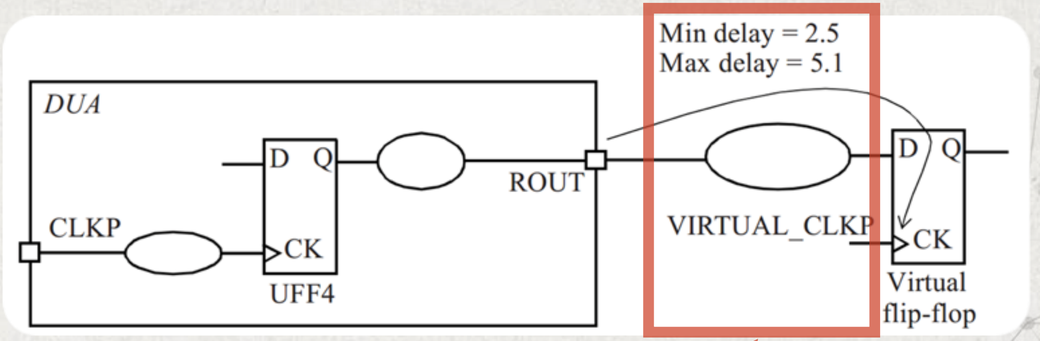


Flip-flop to Output Path




```
Startpoint: UFF4 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: ROUT (output port clocked by VIRTUAL_CLKP)
  Path Group: VIRTUAL_CLKP
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLKP (rise edge)                   0.00       0.00
  clock source latency                     0.00       0.00
  CLKP (in)                                0.00       0.00 r
  UCKBUF4/C (CKB  )                        0.06       0.06 r
  UCKBUF5/C (CKB  )                        0.06       0.12 r
  UFF4/CK (DFF )                           0.00       0.12 r
  UFF4/Q (DFF )                            0.13       0.25 r
  UBUF3/Z (BUFF  )                         0.09       0.33 r
  ROUT (out)                               0.00       0.33 r
  data arrival time                                   0.33
```

Flip-flop to Output Path

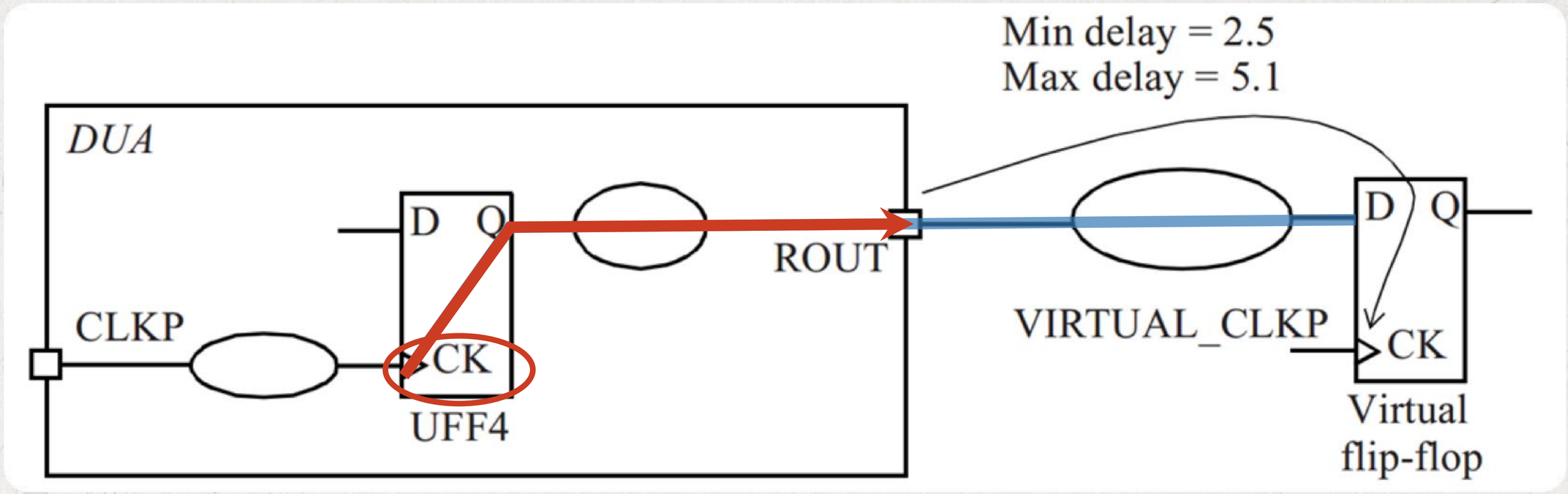


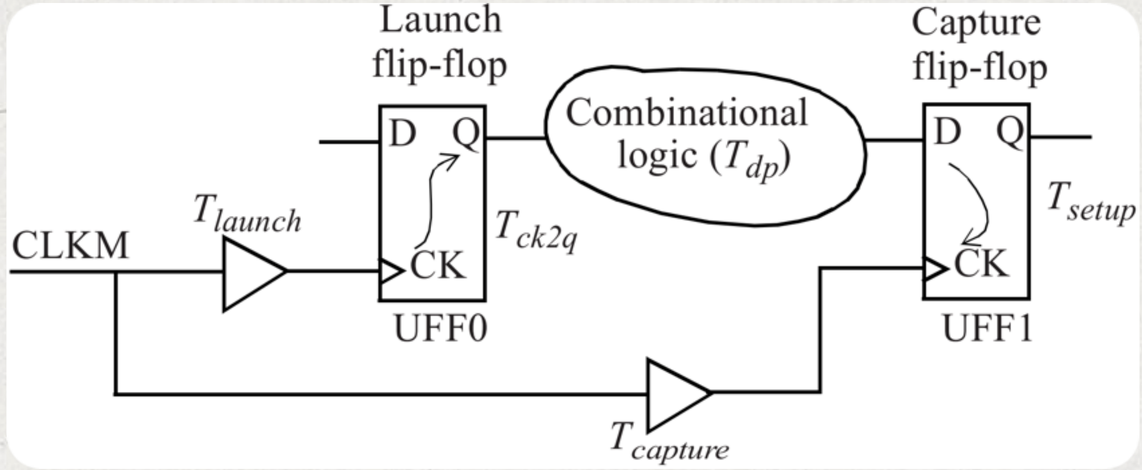
clock VIRTUAL_CLKP (rise edge)	12.00	12.00
clock network delay (ideal)	0.00	12.00
clock uncertainty	-0.30	11.70
output external delay	**-5.10**	6.60
data required time		6.60
data required time		6.60
data arrival time		-0.33
slack (MET)		6.27

Flip-flop to Output Path

正数

clock VIRTUAL_CLKP (rise edge)	12.00	12.00
clock network delay (ideal)	0.00	12.00
clock uncertainty	-0.30	11.70
output external delay	**-5.10**	6.60
data required time		6.60
---		
data required time		6.60
data arrival time		-0.33
---		
slack (MET)		6.27





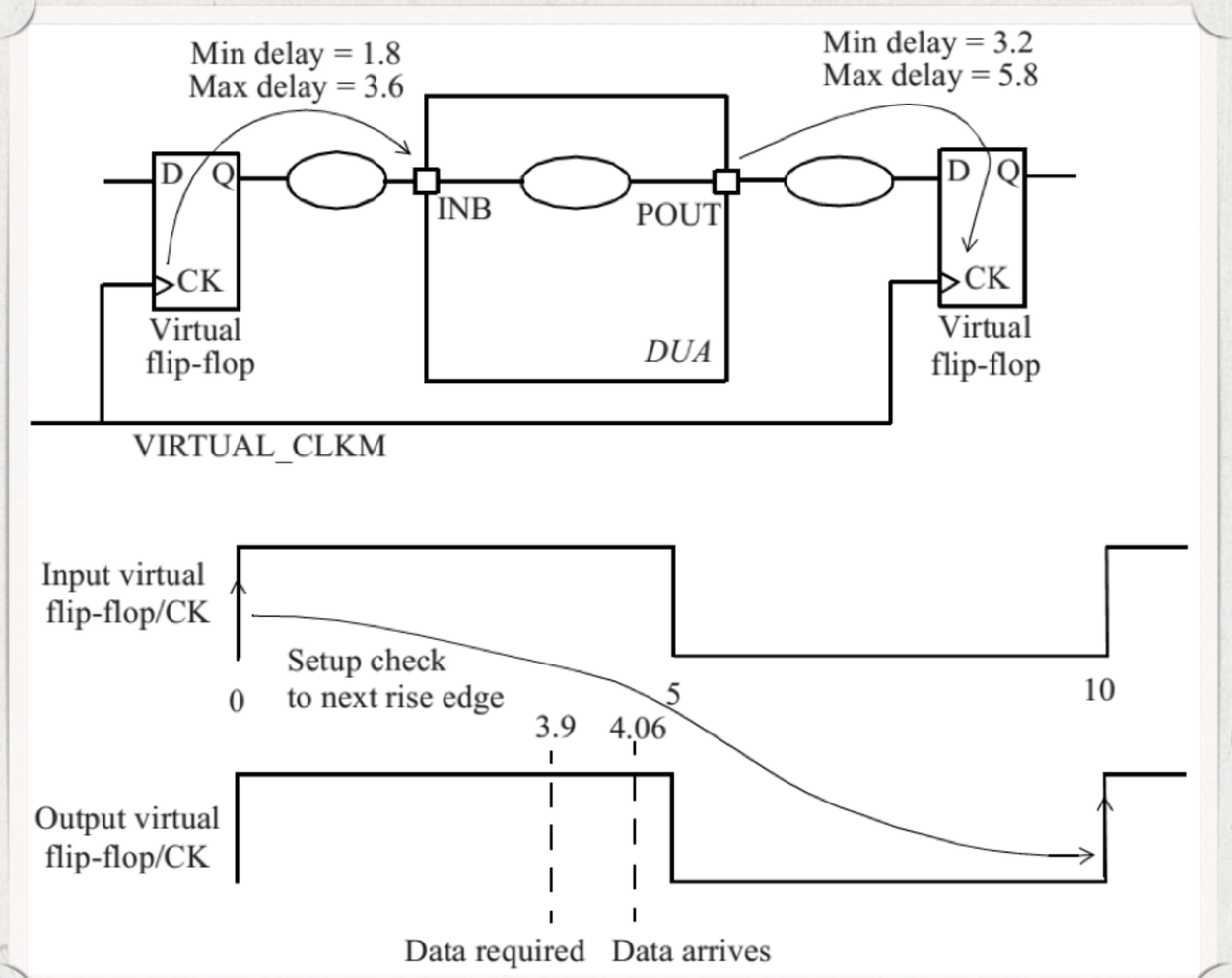
$$T_{launch} + T_{ck2q} + T_{dp} < T_{capture} + T_{cycle} - T_{setup}$$

$$slack = (T_{capture} + T_{cycle} - T_{setup} - T_{uncertainty}) - (T_{launch} + T_{ck2q} + T_{dp})$$

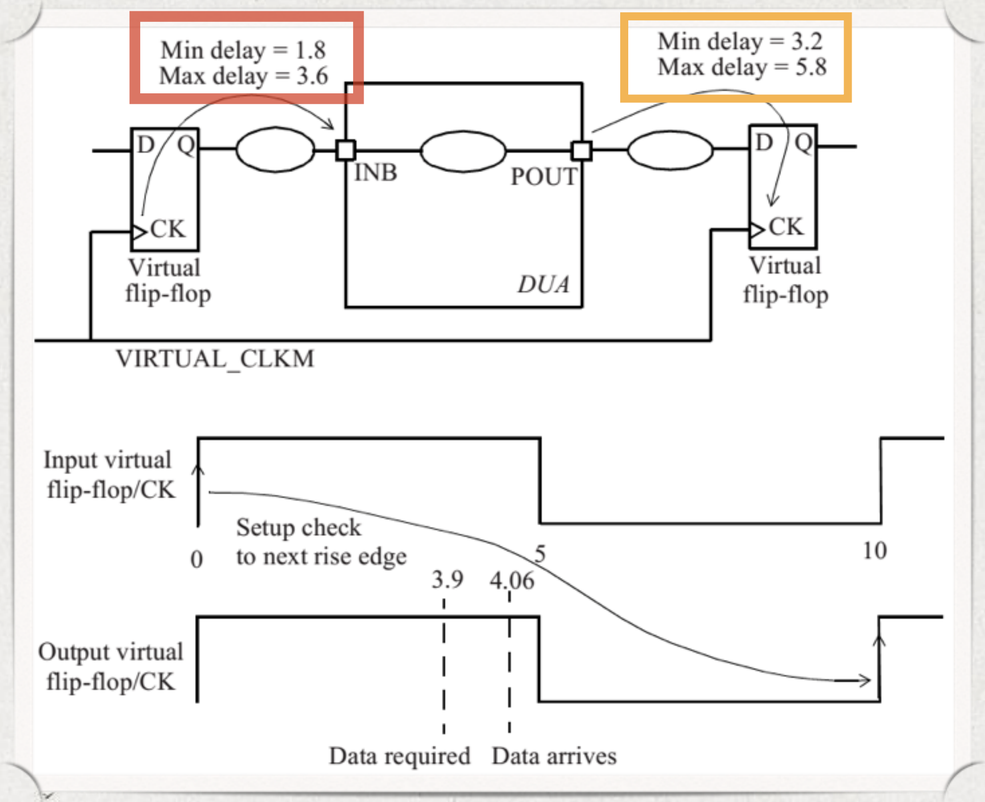
$$slack = (T_{capture} + T_{cycle} - T_{uncertainty} - T_{setup} - T_{output\_delay}) - (T_{launch} + T_{ck2q} + T_{dp})$$

$$\underbrace{0 + 12 - 0.3 - 5.10}_{\text{Data required time}} - \underbrace{0.33}_{\text{Data arrival time}} > 0$$

Input to Output Path



Input to Output Path



input port

output port

- Here are the input and output delay specifications.

  set_input_delay–clock VIRTUAL_CLKM \–max 3.6 {get_ports INB}

  set_output_delay–clock VIRTUAL_CLKM \–max 5.8 {get_ports POUT}

Input to Output Path

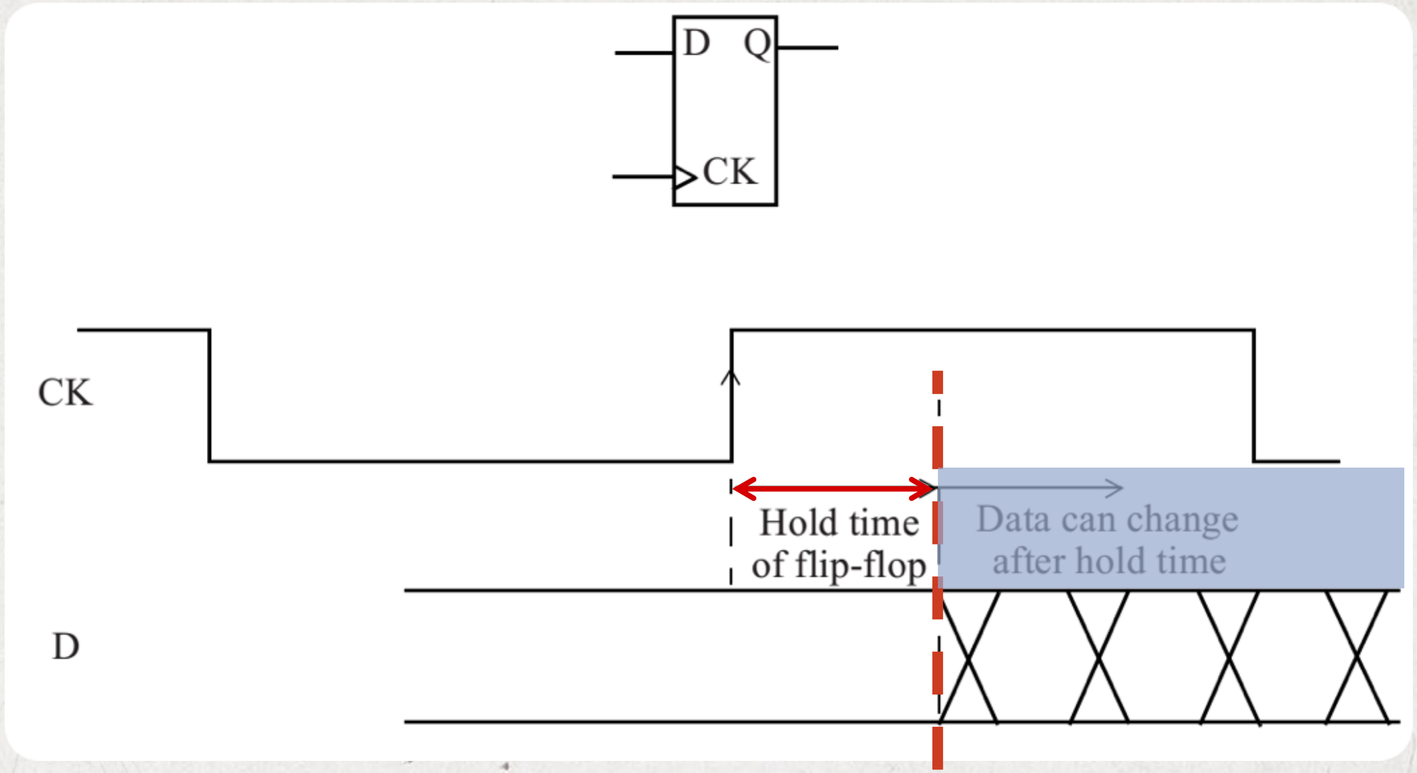
```
Startpoint: INB (input port clocked by VIRTUAL_CLKM)
Endpoint: POUT (output port clocked by VIRTUAL_CLKM)
Path Group: VIRTUAL_CLKM
Path Type: max

Point                                                   Incr       Path
-----------------------------------------------------------------------
clock VIRTUAL_CLKM (rise edge)                          0.00       0.00
clock network delay (ideal)                             0.00       0.00
input external delay                                    3.60       3.60 f
INB (in) <-                                             0.00       3.60 f
UBUF0/Z (BUFF  )                                        0.05       3.65 f
UBUF1/Z (BUFF  )                                        0.06       3.72 f
UINV3/ZN (INV  )                                        0.34       4.06 r
POUT (out)                                              0.00       4.06 r
data arrival time                                                  4.06
```

Input to Output Path

clock VIRTUAL_CLKM (rise edge)	10.00	10.00
clock network delay (ideal)	0.00	10.00
clock uncertainty	-0.30	9.70
output external delay	**-5.80**	3.90
data required time		3.90
data required time		3.90
data arrival time		-4.06
slack (VIOLATED)		-0.16

Hold Timing Check

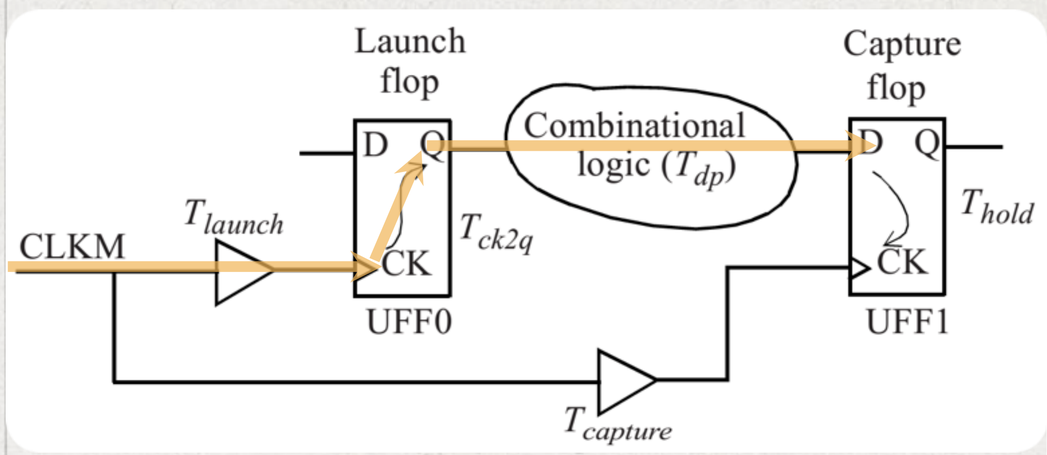
Just like the setup check, a hold timing check is between the launch flipflop - the flip-flop that launches the data, and the capture flip-flop - the flip-flop that captures the data and whose hold time must be satisfied.

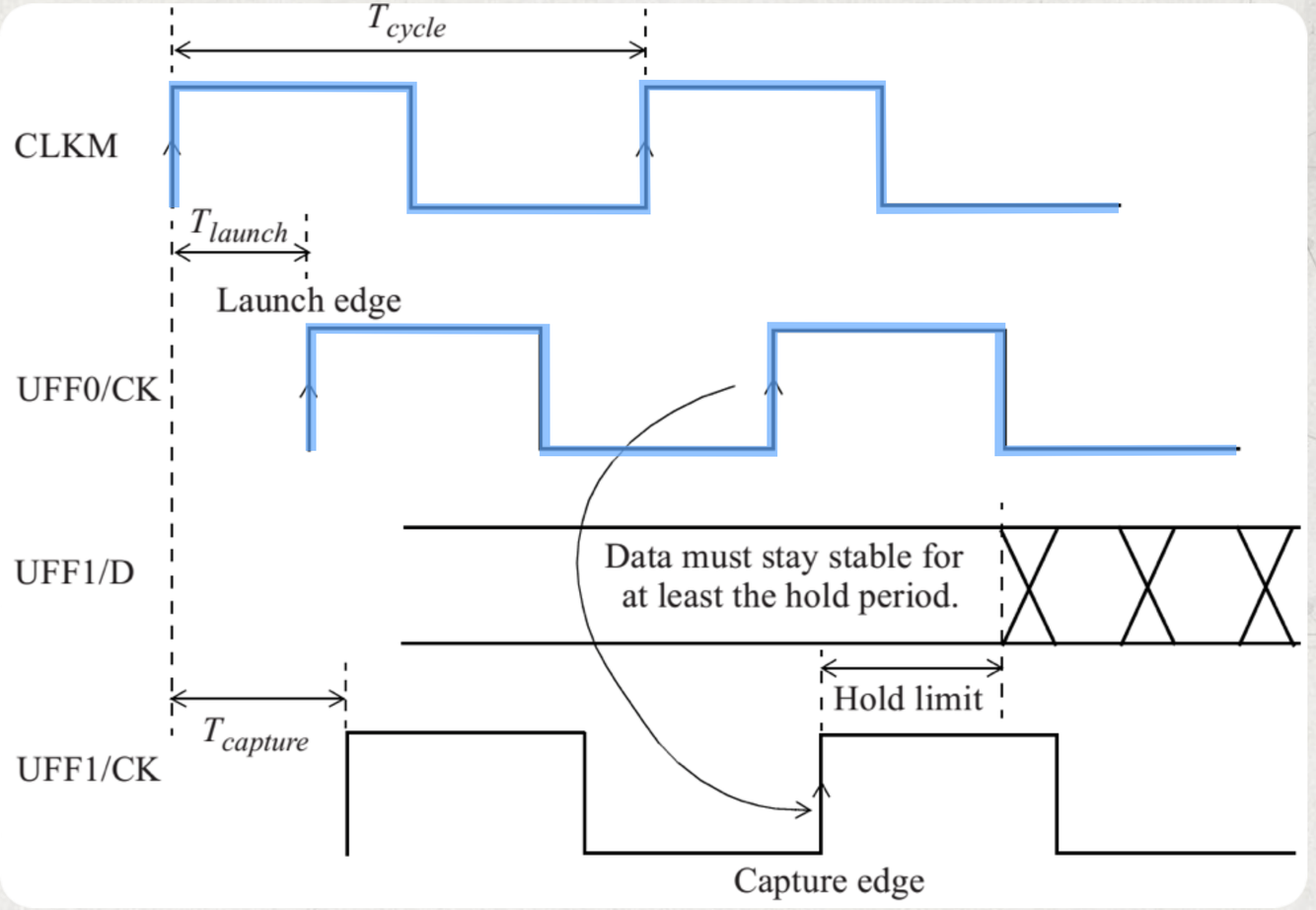


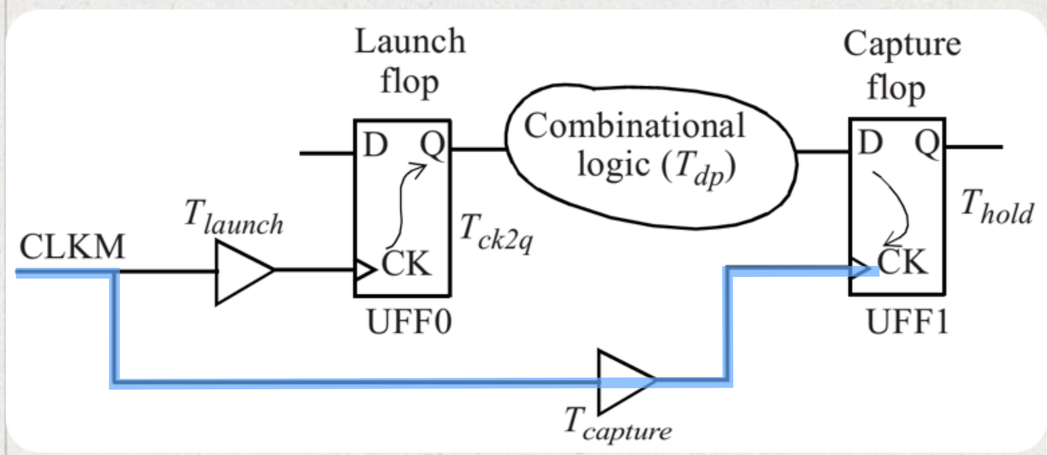
Hold Timing Check

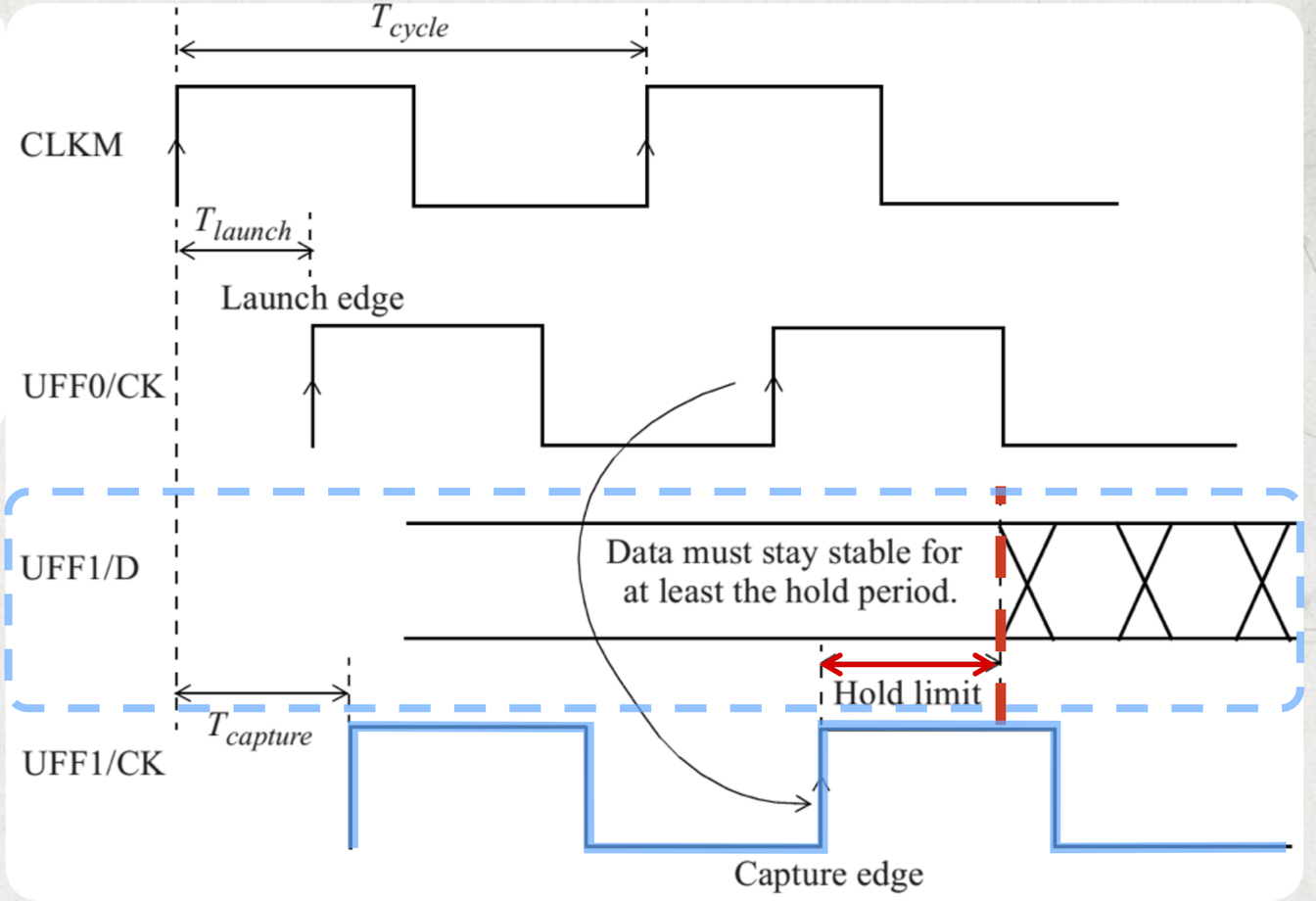
Setup timing check

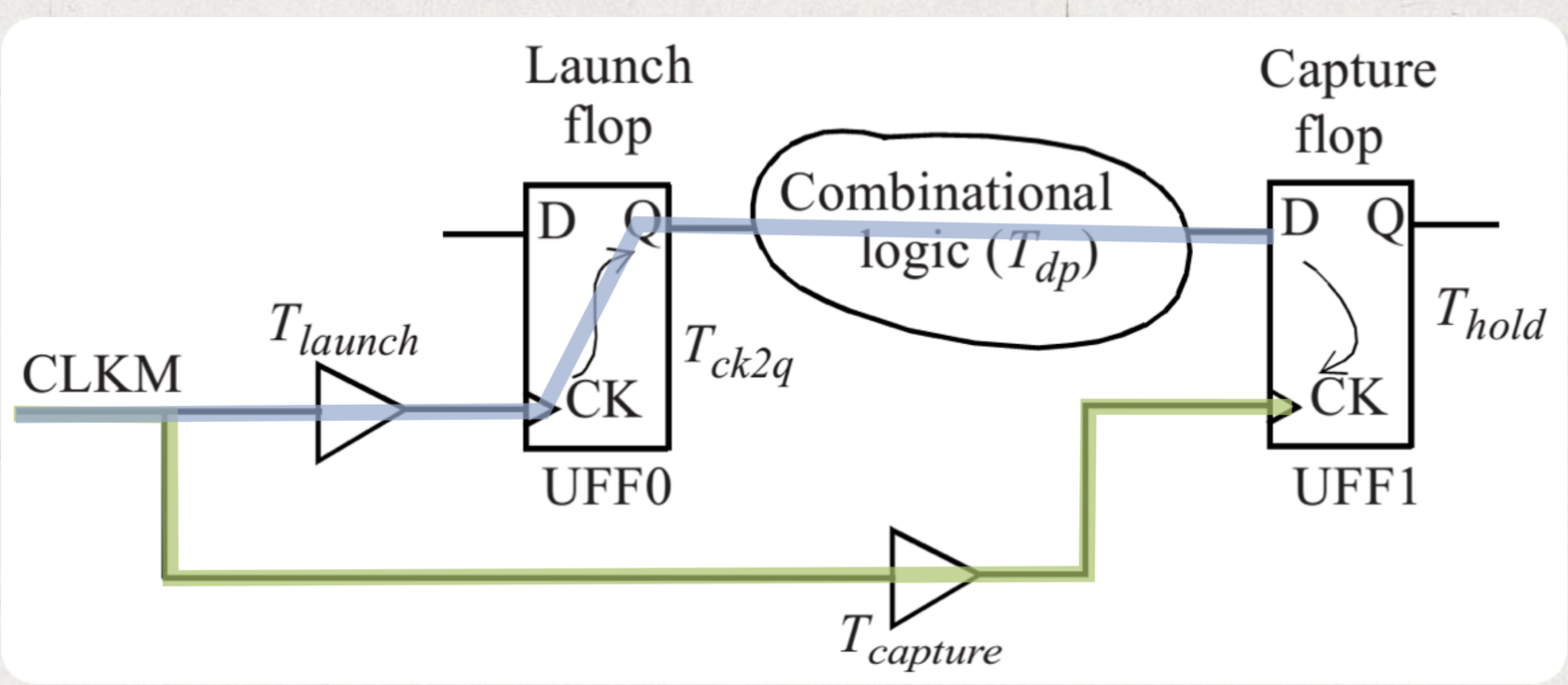
- The hold check is from one active edge of the clock in the launch flip-flop to the same clock edge at the capture flip-flop.
- Thus, a hold check is independent of the clock period.
- The hold check is carried out on each active edge of the clock of the capture flip-flop.


Launch
flop
Capture
flop
D
Q
D
Q
Combinational
logic (T_{dp})
T_{launch}
T_{ck2q}
T_{hold}
CLKM
CK
CK
UFF0
UFF1
$T_{capture}$


T_{cycle}
CLKM
T_{launch}
Launch edge
UFF0/CK
UFF1/D
Data must stay stable for
at least the hold period.
Hold limit
$T_{capture}$
UFF1/CK
Capture edge


Launch
flop
Capture
flop
Combinational
logic (T_{dp})
D
Q
CK
T_{launch}
T_{ck2q}
T_{hold}
CLKM
UFF0
UFF1
$T_{capture}$


T_{cycle}
CLKM
T_{launch}
Launch edge
UFF0/CK
UFF1/D
Data must stay stable for
at least the hold period.
Hold limit
$T_{capture}$
UFF1/CK
Capture edge

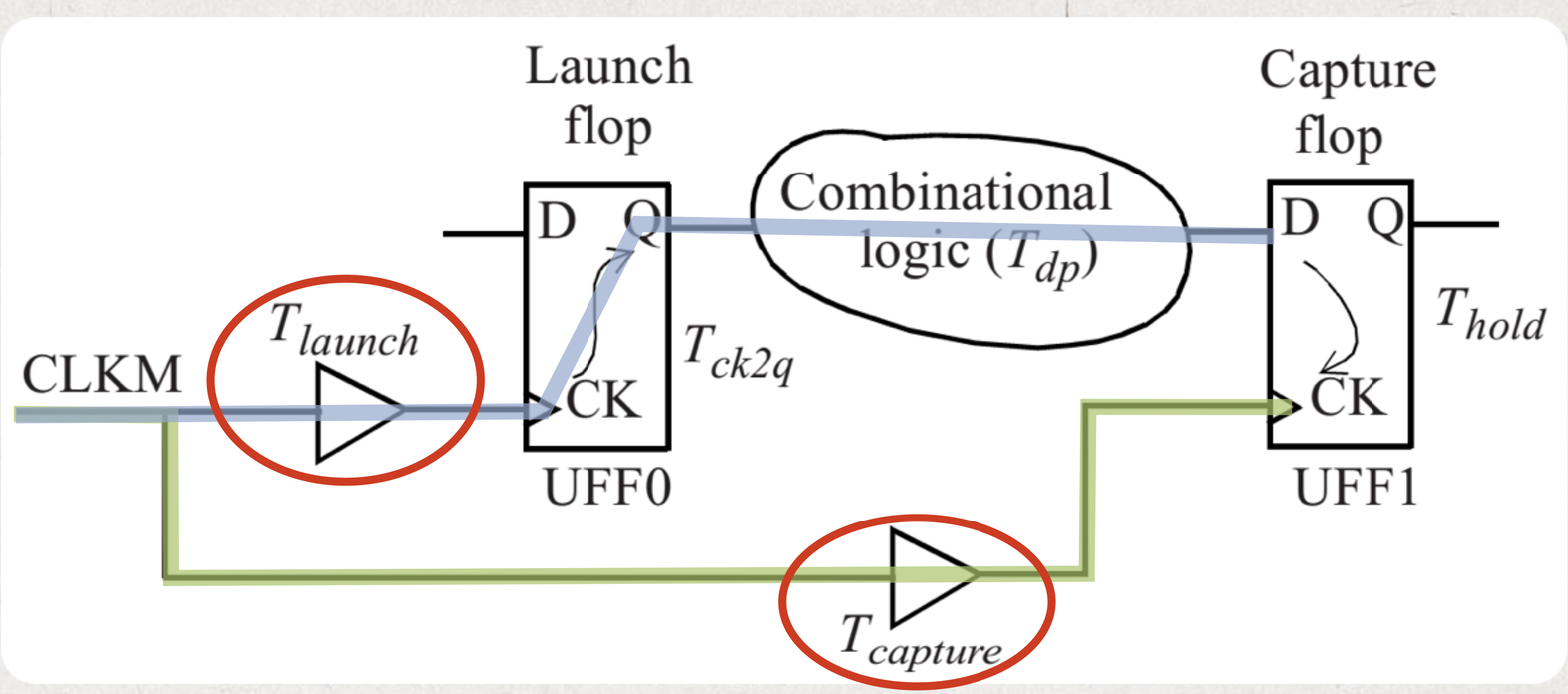


The hold check can be mathematically expressed as:

$$T_{launch} + T_{ck2q} + T_{dp} > T_{capture} + T_{hold}$$

时钟周期

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: min

  Point                                              Incr       Path
  ----------------------------------------------------------------------
  clock CLKM (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKM (in)                                          0.00       0.00 r
  UCKBUF0/C (CKB  )                                  0.06       0.06 r
  UCKBUF1/C (CKB  )                                  0.06       0.11 r
  UFF0/CK (DFF )                                     0.00       0.11 r
  UFF0/Q (DFF ) <-                                   0.14       0.26 r
  UNOR0/ZN (NR2  )                                   0.02       0.28 f
  UBUF4/Z (BUFF  )                                   0.06       0.33 f
  UFF1/D (DFF )                                      0.00       0.33 f
  data arrival time                                             0.33
```



The hold check can be mathematically expressed as:

取最小值

$$T_{launch} + T_{ck2q} + T_{dp} \geq T_{capture} + T_{hold}$$

clock CLKM (rise edge)	**0.00**	0.00	
clock source latency	0.00	0.00	
CLKM (in)	0.00	0.00	r
UCKBUF0/C (CKB)	0.06	0.06	r
UCKBUF2/C (CKB)	0.07	0.12	r
UFF1/CK (DFF)	0.00	0.12	r
clock uncertainty	0.05	0.17	
library hold time	**0.01**	0.19	
data required time		0.19	
data required time		0.19	
data arrival time		-0.33	
slack (MET)		0.14	

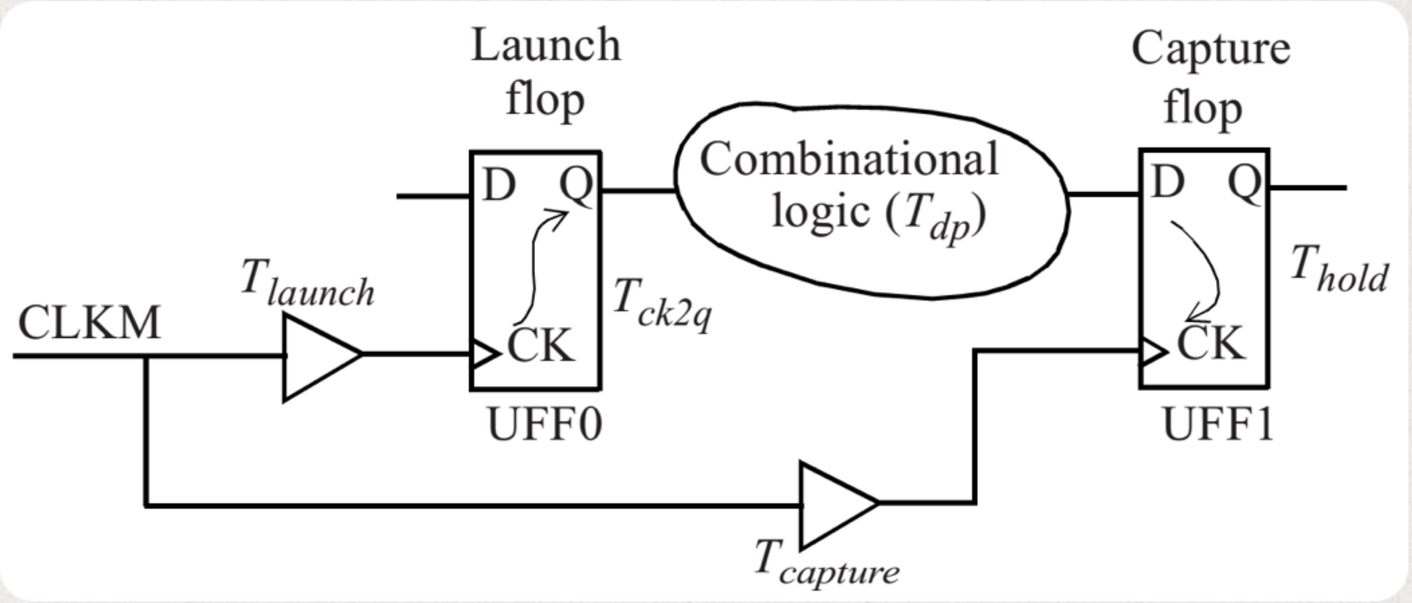
建立时间

要求到达的时间

减去

实际到达的时间

大于0



$$T_{\text{launch}} + T_{\text{ck2q}} + T_{\text{dp}} > T_{\text{capture}} + T_{\text{hold}}$$

$$\text{slack} = (T_{\text{launch}} + T_{\text{ck2q}} + T_{\text{dp}}) - (T_{\text{capture}} + T_{\text{hold}})$$

0.33 − 0.19 > 0

Data required time − Data arrival time > 0

Hold Slack Calculation：

- An interesting point to note is the difference in the way the slack is computed for setup and hold timing reports.

- In the setup timing reports, the arrival time and the required time are computed and the slack is computed to be the required time minus arrival time.