芯动力——硬件加速设计方法

第五章 静态时序分析(4)

邸志雄@西南交通大学

zxdi@home.swjtu.edu.cn

Slow to Fast Clock Domains

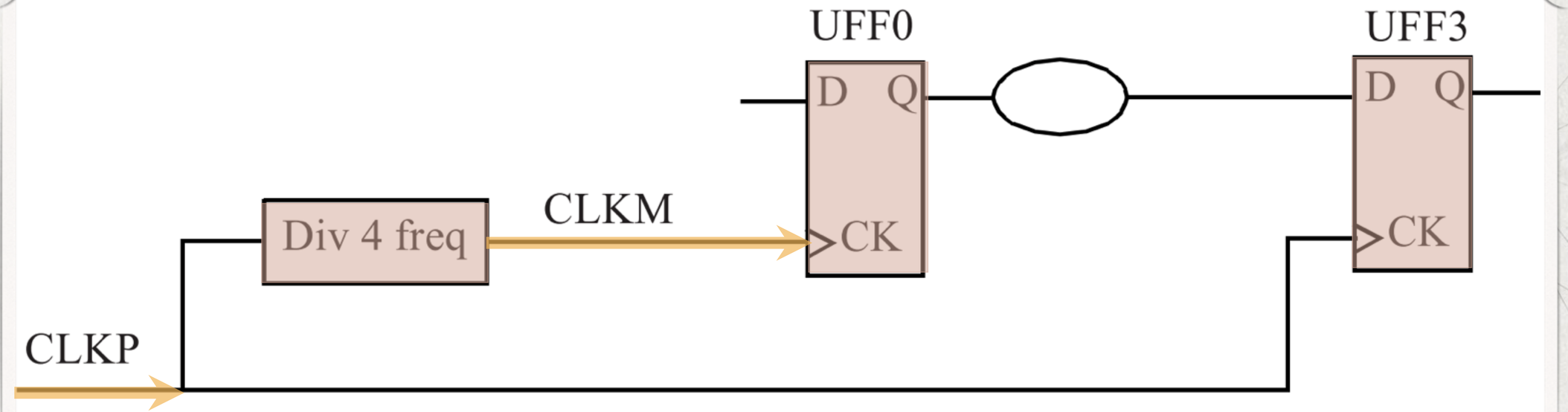


Figure 8-22 *Path from a slow clock to a faster clock.*

Slow to Fast Clock Domains

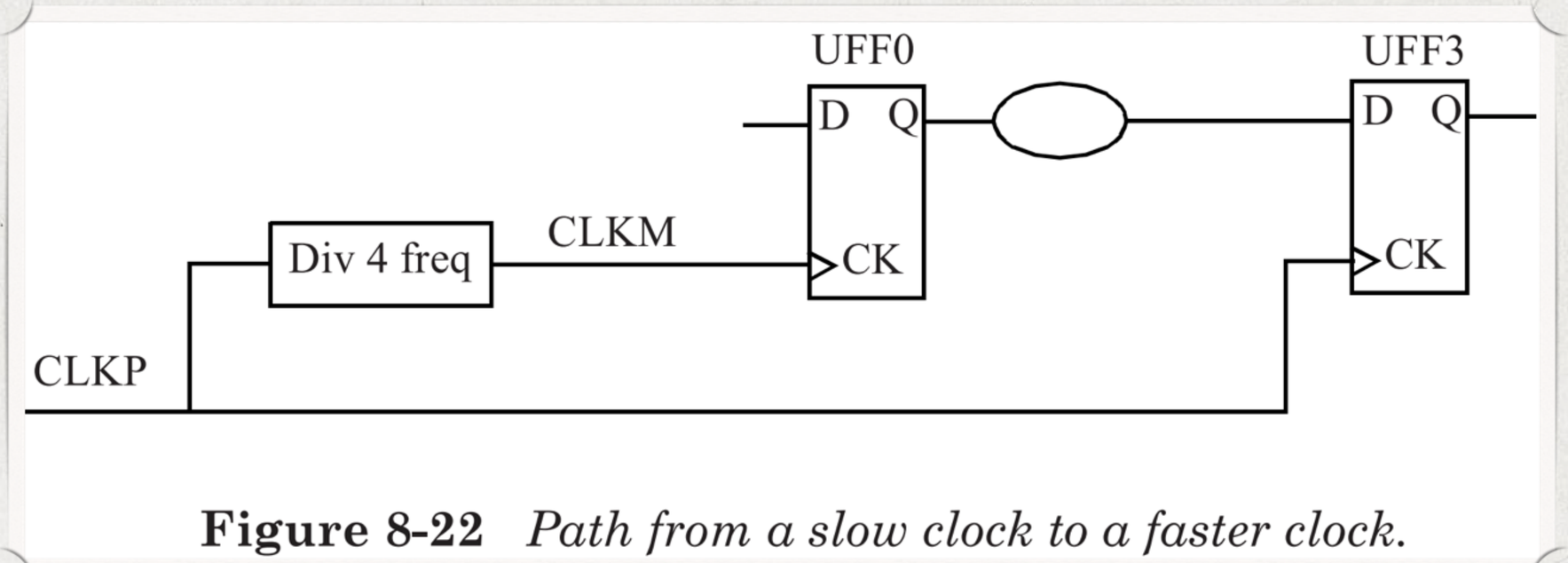


Figure 8-22 *Path from a slow clock to a faster clock.*

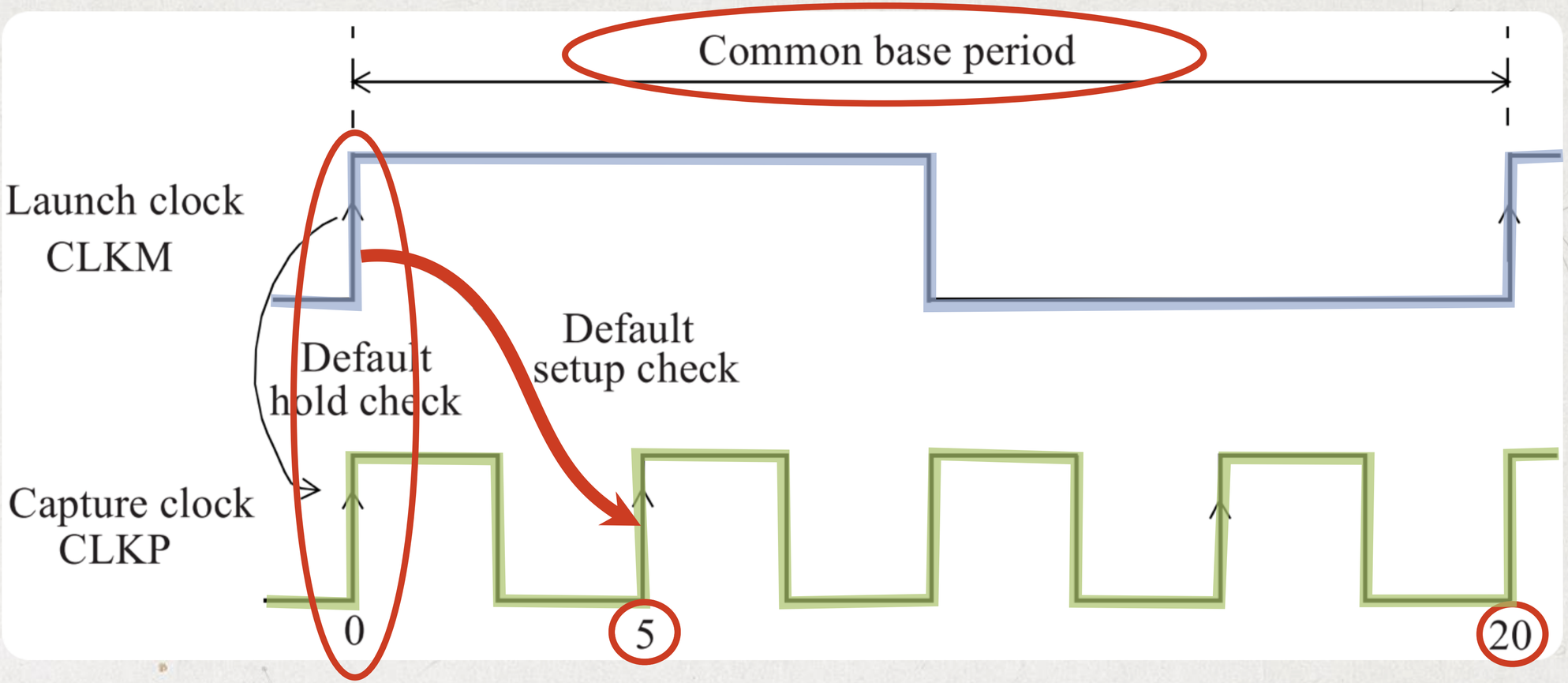
- Here are the clock definitions for our example.

```
create_clock -name CLKM -period 20 -waveform {0 10} [get_ports CLKM]
create_clock -name CLKP -period 5 -waveform {0 2.5} [get_ports CLKP]
```

Slow to Fast Clock Domains

- When the clock frequencies are different for the launch flip-flop and the capture flip-flop, STA is performed by first determining a common base period.
- An example of a message produced when STA is performed on such a design with the above two clocks is given below.
- The faster clock is expanded so that a common period is obtained.

Slow to Fast Clock Domains



Slow to Fast Clock Domains

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------
  clock CLKM (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKM (in)                                          0.00       0.00 r
  UCKBUF0/C (CKB  )                                  0.06       0.06 r
  UCKBUF1/C (CKB  )                                  0.06       0.11 r
  UFF0/CK (DFF )                                     0.00       0.11 r
  UFF0/Q (DFF ) <-                                   0.14       0.26 f
  UNAND0/ZN (ND2  )                                  0.03       0.29 r
  UFF3/D (DFF )                                      0.00       0.29 r
  data arrival time                                             0.29
```

- Notice that the launch clock is at time 0ns while the capture clock is at time 5ns.

clock CLKP (rise edge)	**5.00**	5.00	
clock source latency	0.00	5.00	
CLKP (in)	0.00	5.00	r
UCKBUF4/C (CKB)	0.07	5.07	r
UFF3/CK (DFF)	0.00	5.07	r
clock uncertainty	-0.30	4.77	
library **setup** time	-0.04	4.72	
data required time		4.72	
data required time		4.72	
data arrival time		-0.29	
slack (MET)		4.44	

- As discussed earlier, hold checks are related to the setup checks and ensure that the data launched by a clock edge does not interfere with the previous capture. Here is the hold check timing report.

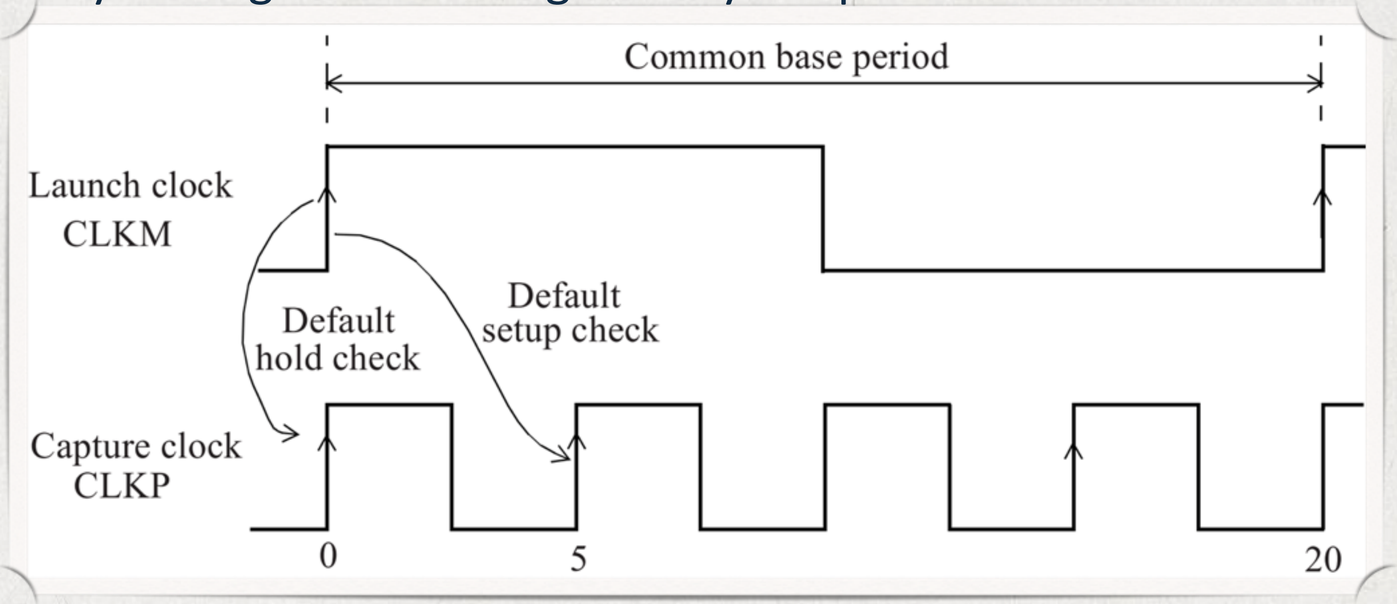
```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
Path Group: CLKP
Path Type: min

Point                                                   Incr       Path
-----------------------------------------------------------------------
clock CLKM (rise edge)                                  0.00       0.00
clock source latency                                    0.00       0.00
CLKM (in)                                               0.00       0.00 r
UCKBUF0/C (CKB  )                                       0.06       0.06 r
UCKBUF1/C (CKB  )                                       0.06       0.11 r
UFF0/CK (DFF )                                          0.00       0.11 r
UFF0/Q (DFF ) <-                                        0.14       0.26 r
UNAND0/ZN (ND2  )                                       0.03       0.29 f
UFF3/D (DFF )                                           0.00       0.29 f
data arrival time                                                  0.29
```

- As discussed earlier, hold checks are related to the setup checks and ensure that the data launched by a clock edge does not interfere with the previous capture. Here is the

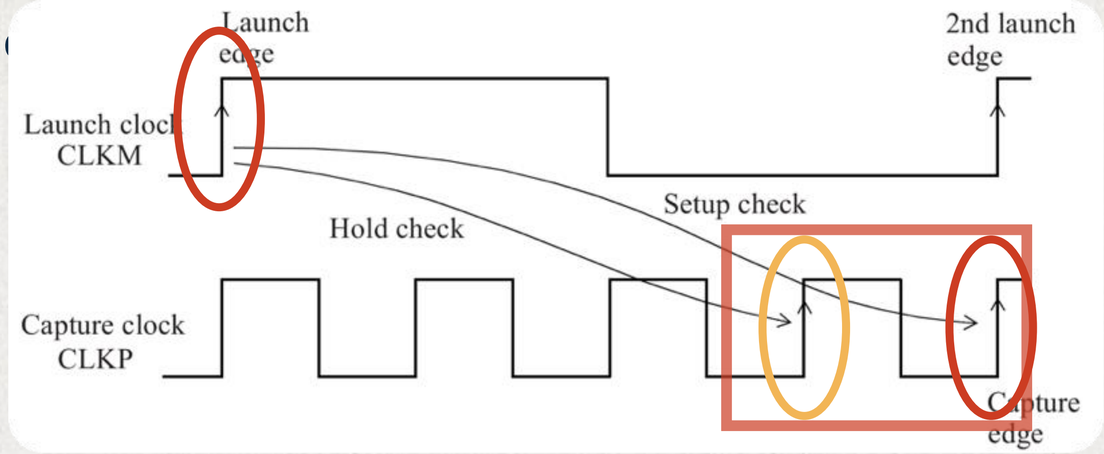
clock CLKP (rise edge)	**0.00**	0.00
clock source latency	0.00	0.00
CLKP (in)	0.00	0.00 r
UCKBUF4/C (CKB)	0.07	0.07 r
UFF3/CK (DFF)	0.00	0.07 r
clock uncertainty	0.05	0.12
library **hold** time	0.02	0.13
data required time		0.13
---	---	---
data required time		0.13
data arrival time		-0.29
---	---	---
slack (MET)		0.16

- In the above example, we can see that the launch data is available every fourth cycle of the capture clock.
- Let us assume that the intention is not to capture data on the very next active edge of CLKP, but to capture on every 4th capture edge. This assumption gives the combinational logic between the flip-flops four periods of CLKP to propagate, which is 20ns.
- We can do this by setting the following multicycle specification:

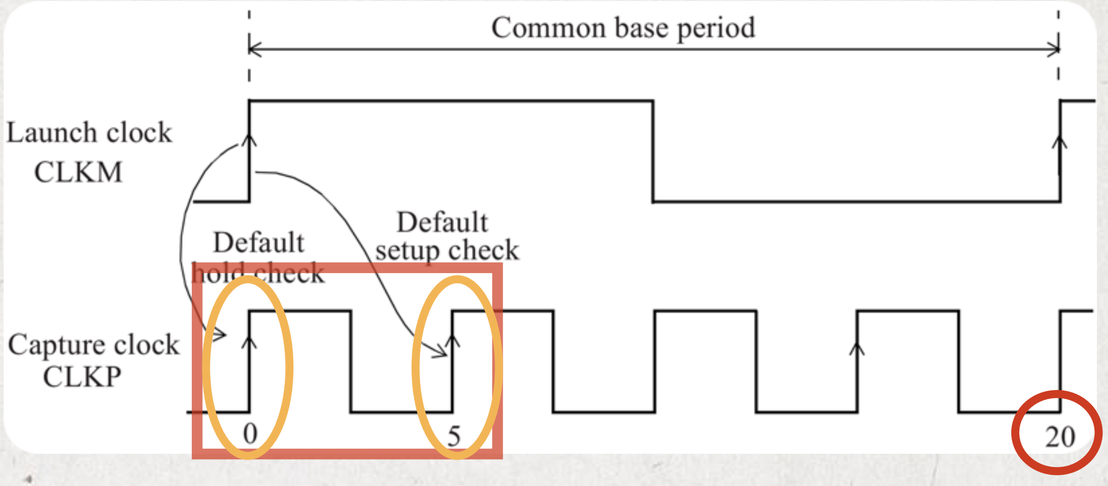


set_multicycle_path 4 -setup -from [get_clocks CLKM] -to [get_clocks CLKP] -end

- The -end specifies that the multicycle of 4 refers to the end point or the capture clock. This multicycle specification changes the setup and hold checks to the



前一个周期的上升沿



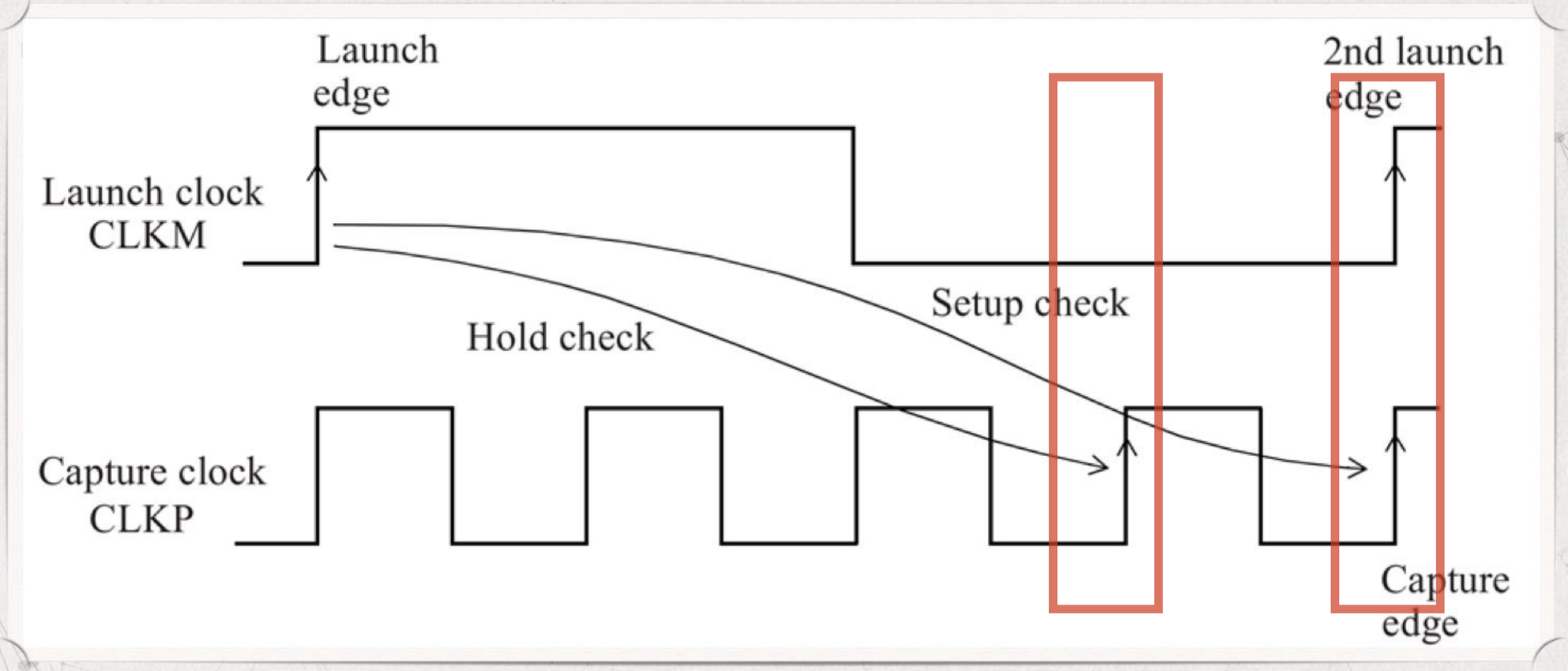
Slow to Fast Clock Domains

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKM (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKM (in)                                          0.00       0.00 r
  UCKBUF0/C (CKB  )                                  0.06       0.06 r
  UCKBUF1/C (CKB  )                                  0.06       0.11 r
  UFF0/CK (DFF )                                     0.00       0.11 r
  UFF0/Q (DFF ) <-                                   0.14       0.26 f
  UNAND0/ZN (ND2  )                                  0.03       0.29 r
  UFF3/D (DFF )                                      0.00       0.29 r
  data arrival time                                             0.29
```

```
clock CLKP (rise edge)                  20.00      20.00
clock source latency                     0.00      20.00
CLKP (in)                                0.00      20.00 r
UCKBUF4/C (CKB  )                        0.07      20.07 r
UFF3/CK (DFF )                           0.00      20.07 r
clock uncertainty                       -0.30      19.77
library setup time                      -0.04      19.72
data required time                                 19.72
-----------------------------------------------------------
data required time                                 19.72
data arrival time                                  -0.29
-----------------------------------------------------------
slack (MET)                                        19.44
```

- Figure shows the hold check - note that the hold check is derived from the setup check and defaults to one cycle preceding the intended capture edge. Here is the hold timing report. Notice that the hold capture edge is at 15ns, one cycle prior to the setup capture



Slow to Fast Clock Domains

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKM (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKM (in)                                          0.00       0.00 r
  UCKBUF0/C (CKB  )                                  0.06       0.06 r
  UCKBUF1/C (CKB  )                                  0.06       0.11 r
  UFF0/CK (DFF )                                     0.00       0.11 r
  UFF0/Q (DFF ) <-                                   0.14       0.26 r
  UNAND0/ZN (ND2  )                                  0.03       0.29 f
  UFF3/D (DFF )                                      0.00       0.29 f
  data arrival time                                             0.29
```

clock CLKP (rise edge)	**15.00**	15.00	
clock source latency	0.00	15.00	
CLKP (in)	0.00	15.00	r
UCKBUF4/C (CKB)	0.07	15.07	r
UFF3/CK (DFF)	0.00	15.07	r
clock uncertainty	0.05	15.12	
library **hold** time	0.02	15.13	
data required time		15.13	
data required time		15.13	
data arrival time		-0.29	
slack (VIOLATED)		-14.84	

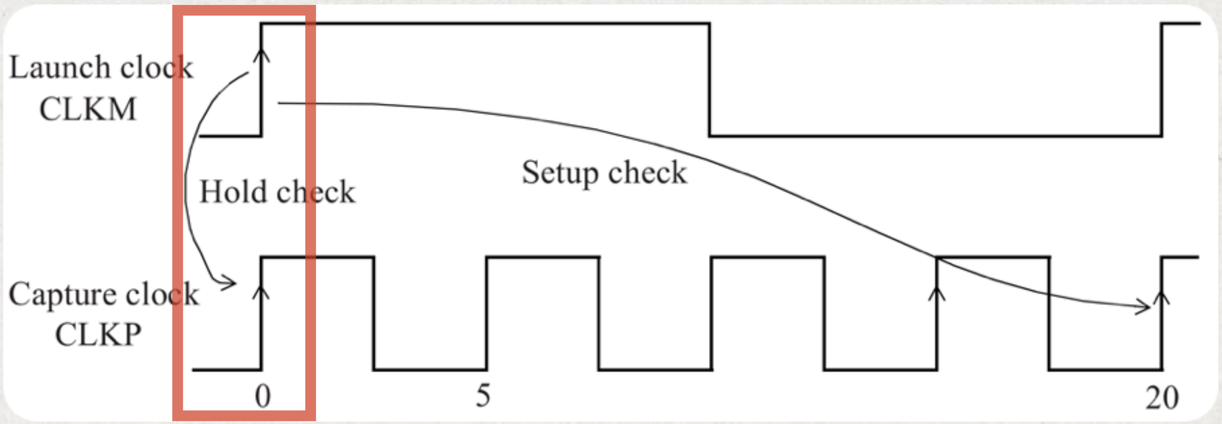
Slow to Fast Clock Domains

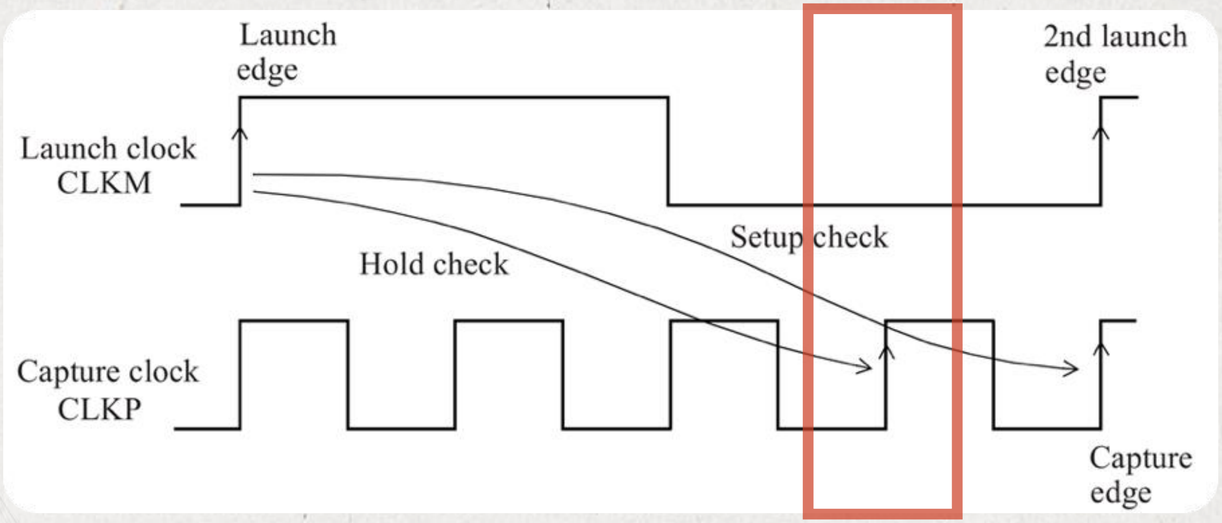
- In most designs, this is not the intended check, and the hold check should be moved all the way back to where the launch edge is. We do this by setting a hold multicycle specification of 3.

```
set_multicycle_path 3 -hold  -from [get_clocks CLKM] -to [get_clocks CLKP] -end
```

- The cycle of 3 moves the hold checking edge back three cycles, that is, to time 0ns. The distinction with a setup multicycle is that in setup, the setup capture edge moves forward by the specified number of cycles from the default setup capture edge; in a hold multicycle, the hold check edge moves backward from the default hold check edge (one cycle before setup edge).

set_multicycle_path 3 -hold -from [get_clocks CLKM] -to [get_clocks CLKP] -end





Slow to Fast Clock Domains

- In summary, if a setup multicycle of N cycles is specified, then most likely a hold multicycle of N-1 cycles should also be specified. A good rule of thumb for multi-frequency multicycle path specification in the case of paths between slow to fast clock domains is to use the -end option. With this option, the setup and hold checks are adjusted based upon the clock cycles of the fast clock.

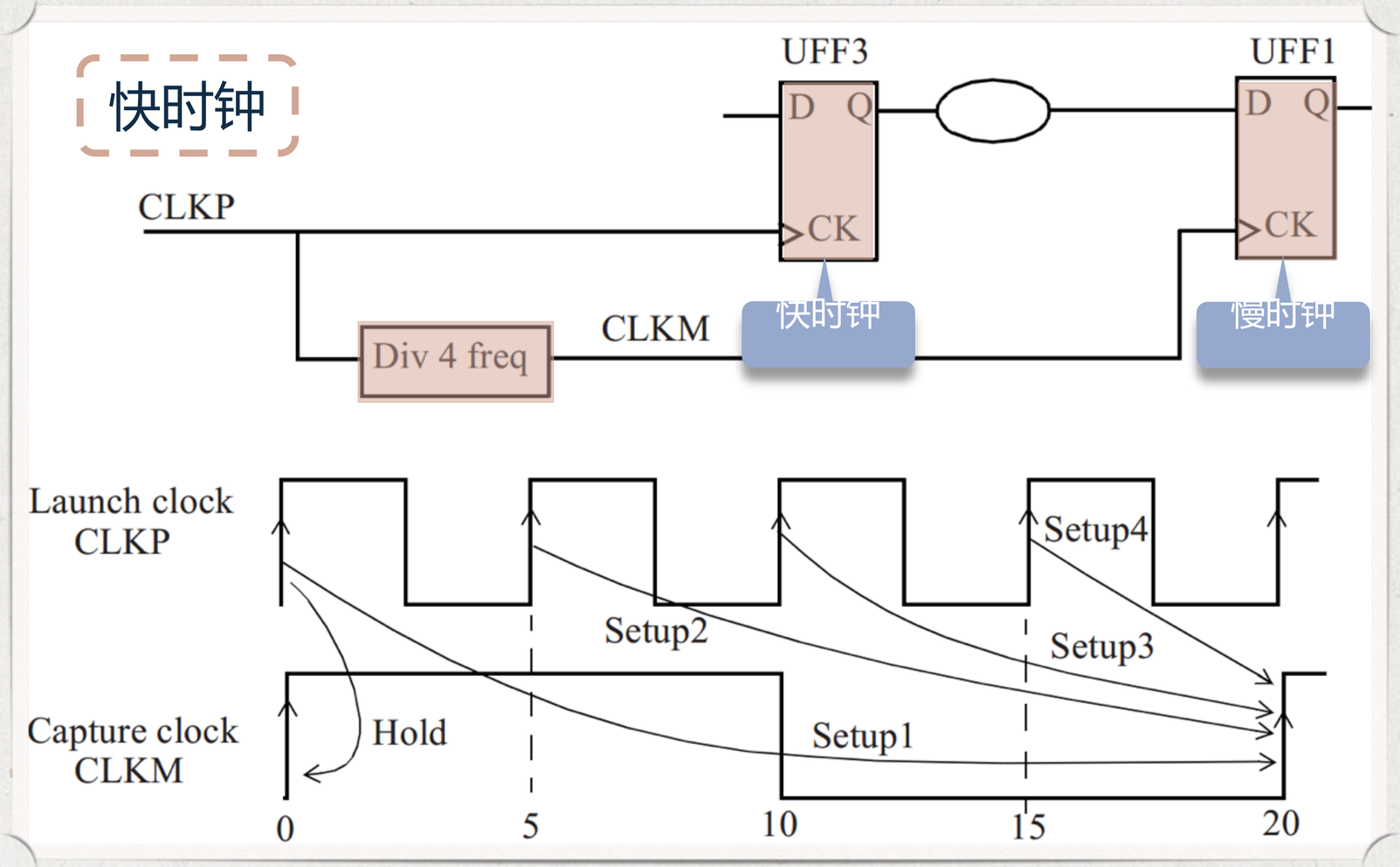
Fast to Slow Clock Domains

- In this subsection, we consider examples where the data path goes from a fast clock domain to a slow clock domain. The default setup and hold checks are as shown in Figure when the following clock definitions are used.

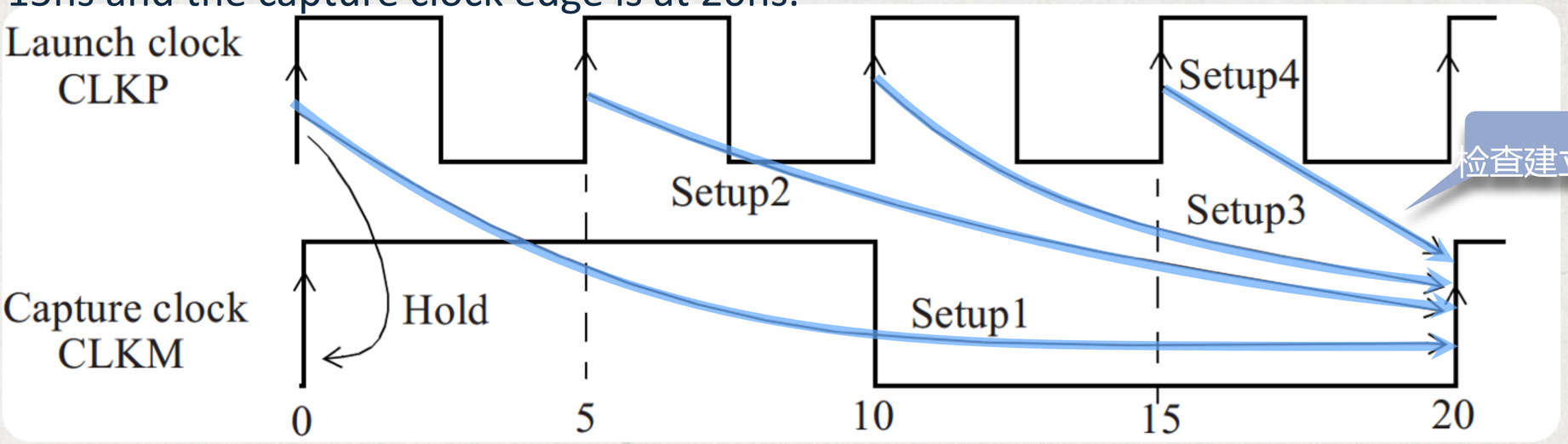
```
create_clock -name CLKP -period 5 -waveform {0 2.5} [get_ports CLKP]
```

```
create_clock -name CLKM -period 20 -waveform {0 10} [get_ports CLKM]
```

Fast to Slow Clock Domains



- There are four setup timing checks possible; see Setup1, Setup2, Setup3 and Setup4 in the figure. However, the most restrictive one is the Setup4 check. Here is the path report of this most restrictive path. Notice that the launch clock edge is at 15ns and the capture clock edge is at 20ns.



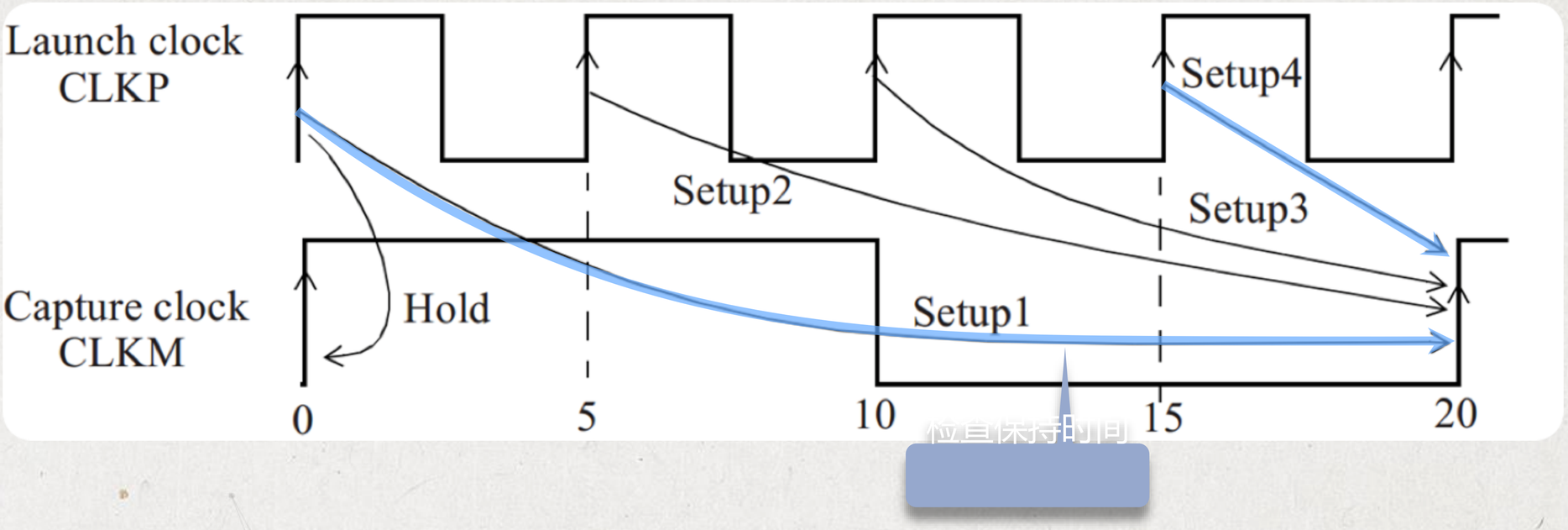
Fast to Slow Clock Domains

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (rise edge)                            15.00      15.00
  clock source latency                               0.00      15.00
  CLKP (in)                                          0.00      15.00 r
  UCKBUF4/C (CKB  )                                  0.07      15.07 r
  UFF3/CK (DFF )                                     0.00      15.07 r
  UFF3/Q (DFF ) <-                                   0.15      15.22 f
  UNOR0/ZN (NR2  )                                   0.05      15.27 r
  UBUF4/Z (BUFF  )                                   0.05      15.32 r
  UFF1/D (DFF )                                      0.00      15.32 r
  data arrival time                                            15.32
```

clock CLKM (rise edge)	**20.00**	20.00	
clock source latency	0.00	20.00	
CLKM (in)	0.00	20.00	r
UCKBUF0/C (CKB)	0.06	20.06	r
UCKBUF2/C (CKB)	0.07	20.12	r
UFF1/CK (DFF)	0.00	20.12	r
clock uncertainty	-0.30	19.82	
library **setup** time	-0.04	19.78	
data required time		19.78	
---	---	---	---
data required time		19.78	
data arrival time		-15.32	
---	---	---	---
slack (MET)		4.46	

- Similar to the setup checks, there are four hold checks possible. Figure shows the most restrictive hold check which ensures that the capture edge at 0ns does not capture the data being launched at 0ns. Here is the timing report for this hold check.



Fast to Slow Clock Domains

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKP (in)                                          0.00       0.00 r
  UCKBUF4/C (CKB  )                                  0.07       0.07 r
  UFF3/CK (DFF )                                     0.00       0.07 r
  UFF3/Q (DFF ) <-                                   0.16       0.22 r
  UNOR0/ZN (NR2  )                                   0.02       0.25 f
  UBUF4/Z (BUFF  )                                   0.06       0.30 f
  UFF1/D (DFF )                                      0.00       0.30 f
  data arrival time                                             0.30
```

clock CLKM (rise edge)	**0.00**	0.00	
clock source latency	0.00	0.00	
CLKM (in)	0.00	0.00	r
UCKBUF0/C (CKB)	0.06	0.06	r
UCKBUF2/C (CKB)	0.07	0.12	r
UFF1/CK (DFF)	0.00	0.12	r
clock uncertainty	0.05	0.17	
library **hold** time	0.01	0.19	
data required time		0.19	
data required time		0.19	
data arrival time		-0.30	
slack (MET)		0.12	

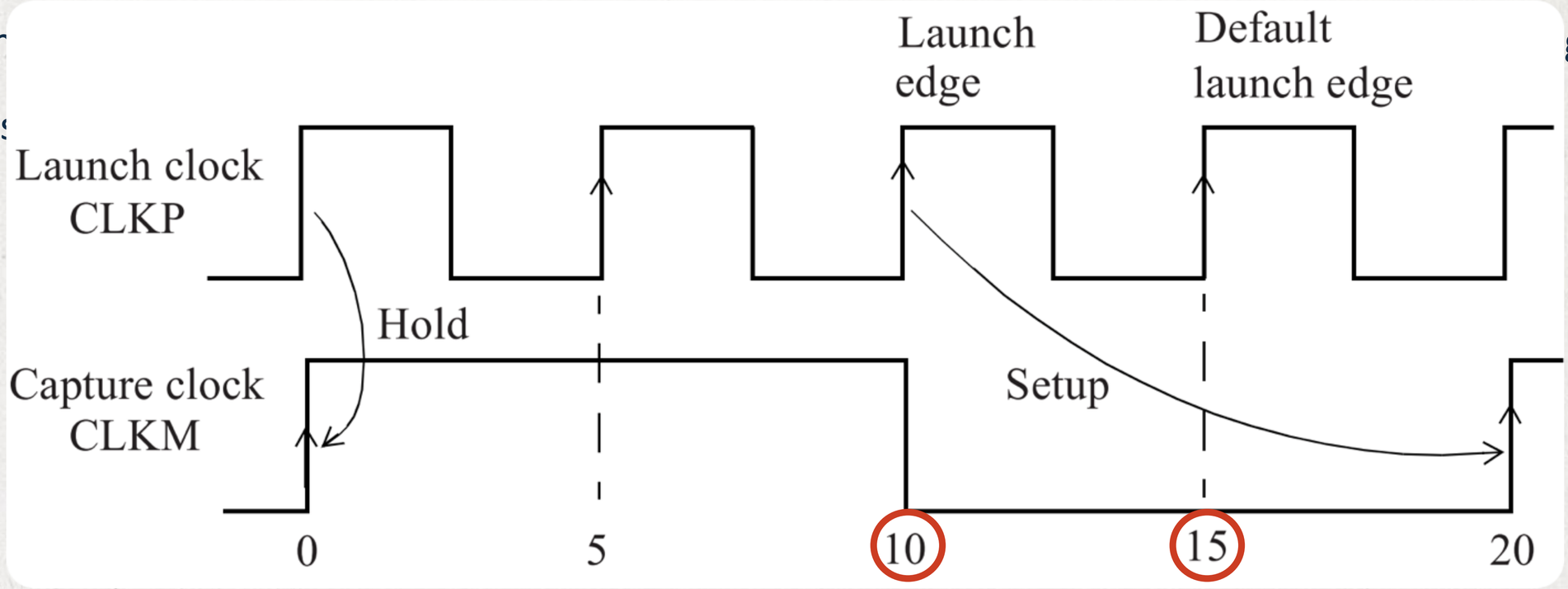
- In general, a designer may specify the data path from the fast clock to the slow clock to be a multicycle path. If the setup check is relaxed to provide two cycles of the faster clock for the data path, the following is included for this multicycle specification:

```
set_multicycle_path 2 -setup -from [get_clocks CLKP] -to [get_clocks CLKM] -start
```

```
set_multicycle_path 1 -hold -from [get_clocks CLKP] -to [get_clocks CLKM] -start
```

- The -start option refers to the launch clock and is the default for a multicycle hold.

- In this case, Figure shows the clock edges used for the setup and hold checks. The -start option specifies that the unit for the number of cycles (2 in this case) is that of the launch clock (CLKP in this case). The setup multicycle of 2 moves the launch edge one edge prior to the default launch edge, that is, at 10ns instead of the default 15ns. The hold multicycle er ge als



- Here is the setup path report. As expected, the launch clock edge is at 10ns and the capture clock edge is at 20ns.

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (rise edge)                           10.00      10.00
  clock source latency                              0.00      10.00
  CLKP (in)                                         0.00      10.00 r
  UCKBUF4/C (CKB  )                                 0.07      10.07 r
  UFF3/CK (DFF )                                    0.00      10.07 r
  UFF3/Q (DFF ) <-                                  0.15      10.22 f
  UNOR0/ZN (NR2  )                                  0.05      10.27 r
  UBUF4/Z (BUFF  )                                  0.05      10.32 r
  UFF1/D (DFF )                                     0.00      10.32 r
  data arrival time                                           10.32
```

- Here is the setup path report. As expected, the launch clock edge is at 10ns and the capture clock edge is at 20ns.

```
clock CLKM (rise edge)                          20.00      20.00
clock source latency                             0.00      20.00
CLKM (in)                                        0.00      20.00 r
UCKBUF0/C (CKB  )                                0.06      20.06 r
UCKBUF2/C (CKB  )                                0.07      20.12 r
UFF1/CK (DFF )                                   0.00      20.12 r
clock uncertainty                               -0.30      19.82
library setup time                              -0.04      19.78
data required time                                         19.78
-----------------------------------------------------------------
data required time                                         19.78
data arrival time                                         -10.32
-----------------------------------------------------------------
slack (MET)                                                9.46
```

- Here is the hold path timing report. The hold check is at 0ns where both the capture and launch clocks have rising edges

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKP (in)                                          0.00       0.00 r
  UCKBUF4/C (CKB  )                                  0.07       0.07 r
  UFF3/CK (DFF )                                     0.00       0.07 r
  UFF3/Q (DFF ) <-                                   0.16       0.22 r
  UNOR0/ZN (NR2  )                                   0.02       0.25 f
  UBUF4/Z (BUFF  )                                   0.06       0.30 f
  UFF1/D (DFF )                                      0.00       0.30 f
  data arrival time                                             0.30
```

- Here is the hold path timing report. The hold check is at 0ns where both the capture and launch clocks have rising edges

clock CLKM (rise edge)	**0.00**	0.00	
clock source latency	0.00	0.00	
CLKM (in)	0.00	0.00	r
UCKBUF0/C (CKB)	0.06	0.06	r
UCKBUF2/C (CKB)	0.07	0.12	r
UFF1/CK (DFF)	0.00	0.12	r
clock uncertainty	0.05	0.17	
library **hold** time	0.01	0.19	
data required time		0.19	
data required time		0.19	
data arrival time		-0.30	
slack (MET)		0.12	

Fast to Slow Clock Domains

- Unlike the case of paths from slow to fast clock domains, a good rule of thumb for multi-frequency multicycle path specification in the case of paths from fast to slow clock domains is to use the -start option. The setup and hold checks are then adjusted based upon the fast clock.