芯动力——硬件加速设计方法

第五章 静态时序分析(5)

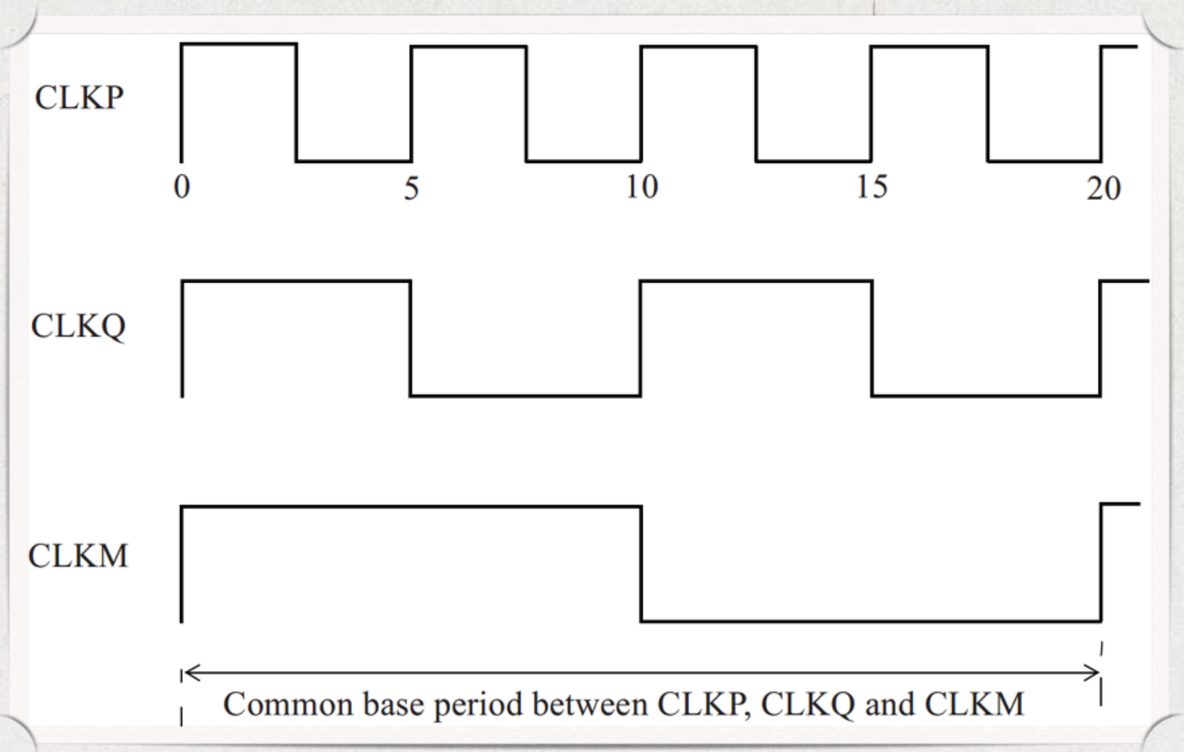
邸志雄@西南交通大学

zxdi@home.swjtu.edu.cn

Multiple Clocks

1- Integer Multiples

- Often there are multiple clocks defined in a design with frequencies that are simple (or integer) multiples of each other.
- In such cases, STA is performed by computing a common base period among all related clocks (two clocks are related if they have a data path between their domains). The common base period is established so that all clocks are synchronized.

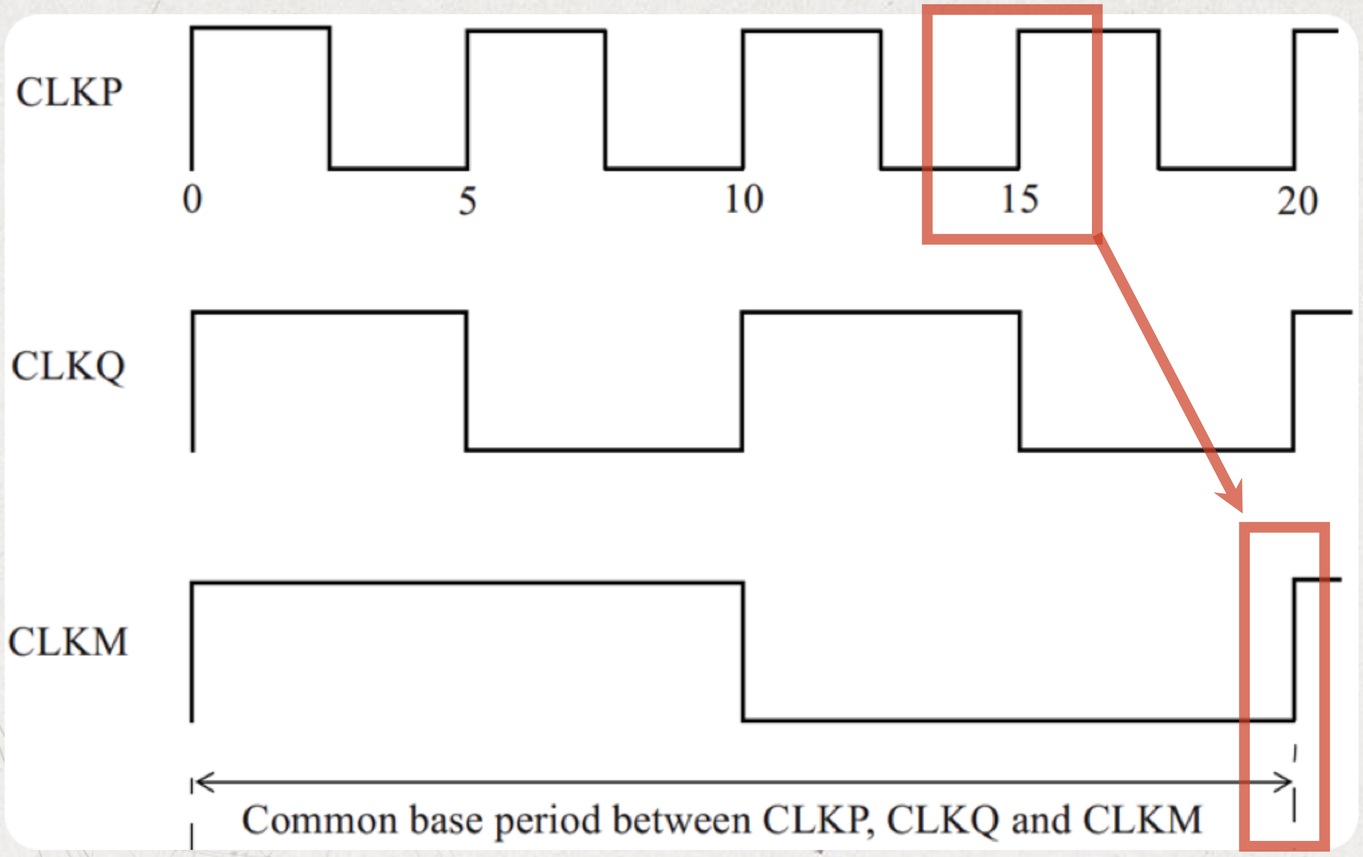


- Here is an example that shows four related clocks:

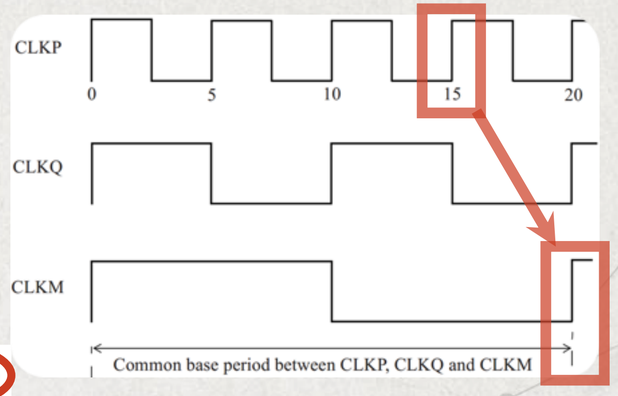
```
create_clock -name CLKP -period 5 -waveform {0 2.5} [get_ports CLKP]

create_clock -name CLKQ -period 10 -waveform {0 5}

create_clock -name CLKM -period 20 -waveform {0 10} [get_ports CLKM]
```

- Here is a setup timing report for a path that goes from the faster clock to the slower clock.

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (rise edge)                            15.00      15.00
  clock source latency                               0.00      15.00
  CLKP (in)                                          0.00      15.00 r
  UCKBUF4/C (CKB  )                                  0.07      15.07 r
  UFF3/CK (DFF )                                     0.00      15.07 r
  UFF3/Q (DFF ) <-                                   0.15      15.22 f
  UNOR0/ZN (NR2  )                                   0.05      15.27 r
  UBUF4/Z (BUFF  )                                   0.05      15.32 r
  UFF1/D (DFF )                                      0.00      15.32 r
  data arrival time                                            15.32
```

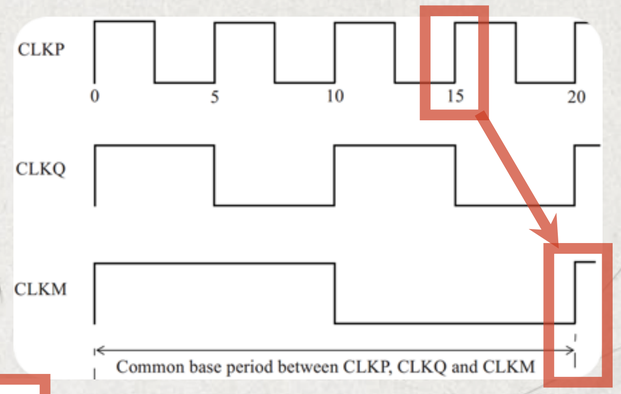


- Here is a setup timing report for a path that goes from the faster clock to the slower clock.




```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLKP (rise edge)                  15.00      15.00
  clock source latency                     0.00      15.00
  CLKP (in)                                0.00      15.00 r
  UCKBUF4/C (CKB  )                        0.07      15.07 r
  UFF3/CK (DFF )                           0.00      15.07 r
  UFF3/Q (DFF ) <-                         0.15      15.22 f
  UNOR0/ZN (NR2  )                         0.05      15.27 r
  UBUF4/Z (BUFF  )                         0.05      15.32 r
  UFF1/D (DFF )                            0.00      15.32 r
  data arrival time                                  15.32
```

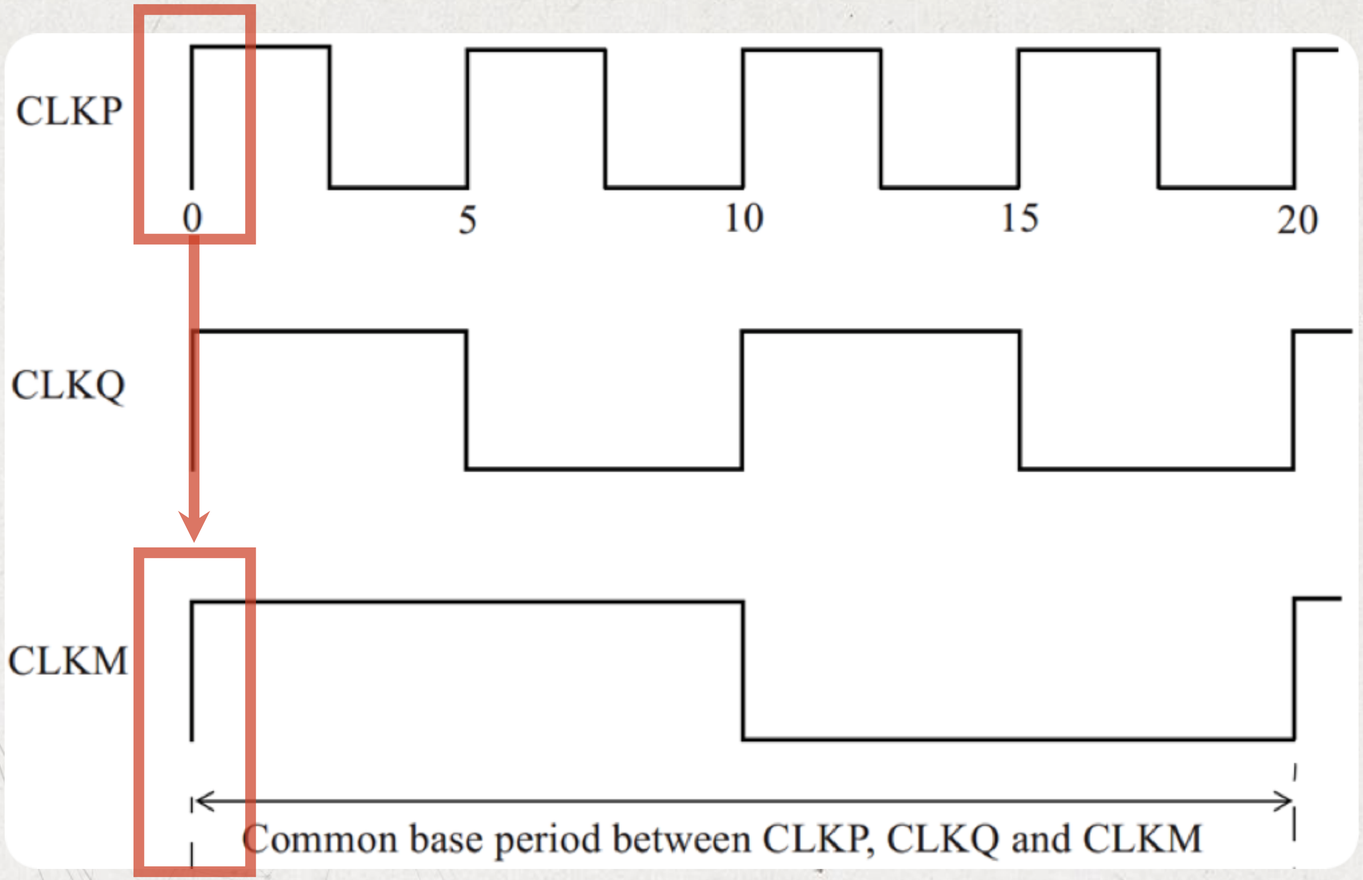
- Here is a setup timing report for a path that goes from the faster clock to the slower clock.



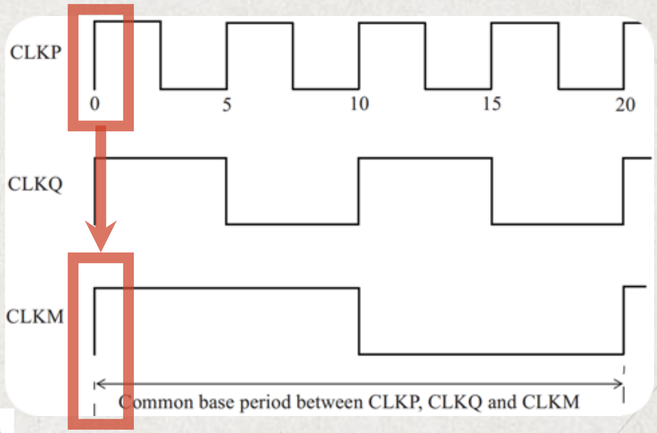
clock CLKM (rise edge)	**20.00**	20.00	
clock source latency	0.00	20.00	
CLKM (in)	0.00	20.00	r
UCKBUF0/C (CKB)	0.06	20.06	r
UCKBUF2/C (CKB)	0.07	20.12	r
UFF1/CK (DFF)	0.00	20.12	r
clock uncertainty	-0.30	19.82	
library **setup** time	-0.04	19.78	
data required time		19.78	
data required time		19.78	
data arrival time		-15.32	
slack (MET)		4.46	

- Here is the corresponding hold path report.

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (rise edge)                            15.00      15.00
  clock source latency                               0.00      15.00
  CLKP (in)                                          0.00      15.00 r
  UCKBUF4/C (CKB  )                                  0.07      15.07 r
  UFF3/CK (DFF )                                     0.00      15.07 r
  UFF3/Q (DFF ) <-                                   0.15      15.22 f
  UNOR0/ZN (NR2  )                                   0.05      15.27 r
  UBUF4/Z (BUFF  )                                   0.05      15.32 r
  UFF1/D (DFF )                                      0.00      15.32 r
  data arrival time                                            15.32
```

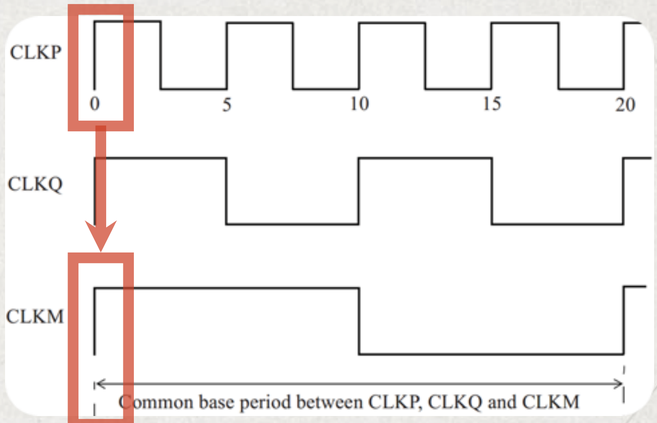


- Here is the corresponding hold path report.




```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: min

Point                                          Incr       Path
-----------------------------------------------------------------
clock CLKP (rise edge)                         0.00       0.00
clock source latency                           0.00       0.00
CLKP (in)                                      0.00       0.00 r
UCKBUF4/C (CKB  )                              0.07       0.07 r
UFF3/CK (DFF )                                 0.00       0.07 r
UFF3/Q (DFF ) <-                               0.16       0.22 r
UNOR0/ZN (NR2  )                               0.02       0.25 f
UBUF4/Z (BUFF  )                               0.06       0.30 f
UFF1/D (DFF )                                  0.00       0.30 f
data arrival time                                         0.30
```

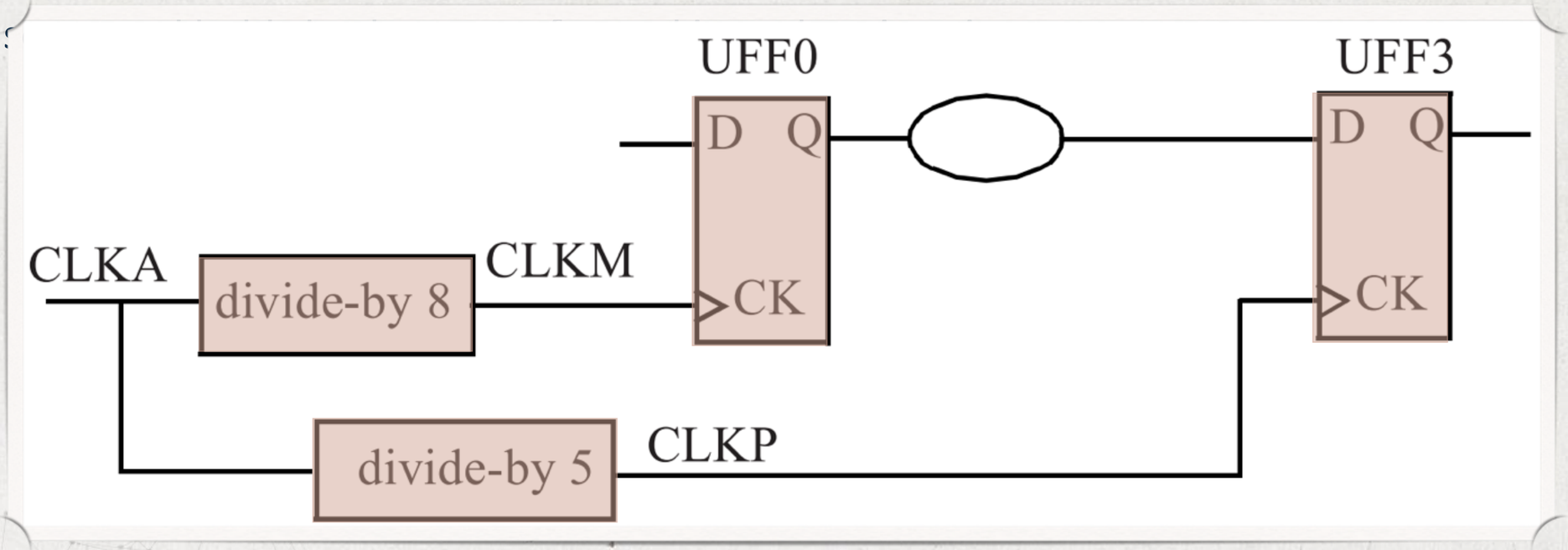
- Here is the corresponding hold path report.



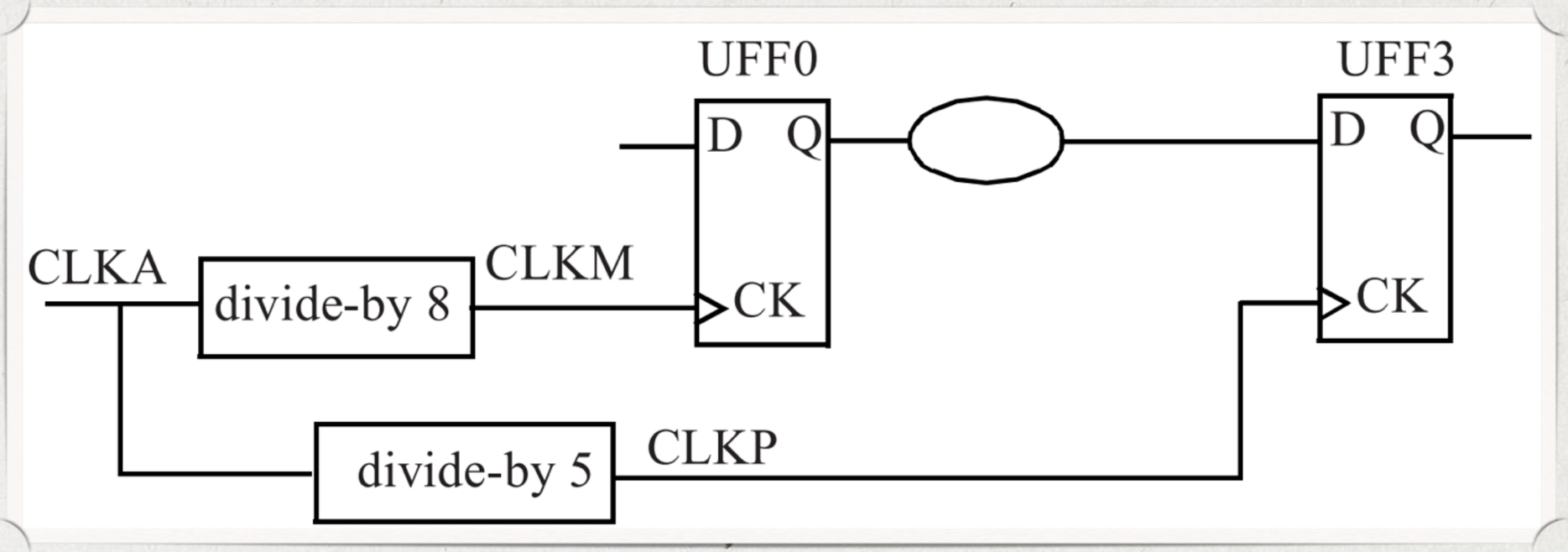

```
clock CLKM (rise edge)                    0.00       0.00
clock source latency                      0.00       0.00
CLKM (in)                                 0.00       0.00 r
UCKBUF0/C (CKB  )                         0.06       0.06 r
UCKBUF2/C (CKB  )                         0.07       0.12 r
UFF1/CK (DFF )                            0.00       0.12 r
clock uncertainty                         0.05       0.17
library hold time                         0.01       0.19
data required time                                   0.19
-----------------------------------------------------------
data required time                                   0.19
data arrival time                                   -0.30
-----------------------------------------------------------
slack (MET)                                          0.12
```

2- Non-Integer Multiples

- Consider the case when there is a data path between two clock domains whose frequencies are not multiples of each other.
- For example, the launch clock is divide-by-8 of a common clock and the capture clock is divide-by-5 of the common clock as shown in Figure. This section describes how the

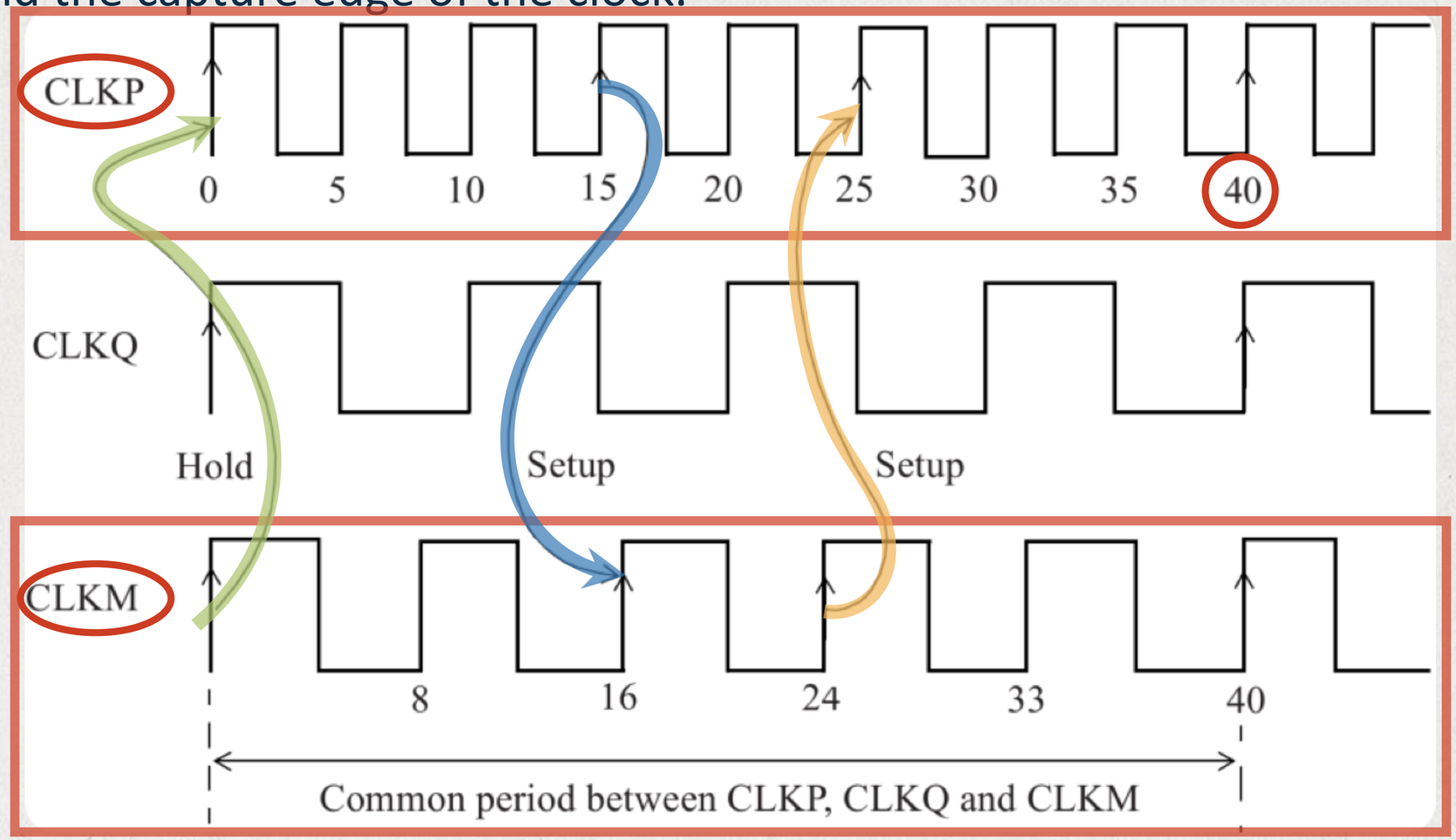


2- Non-Integer Multiples

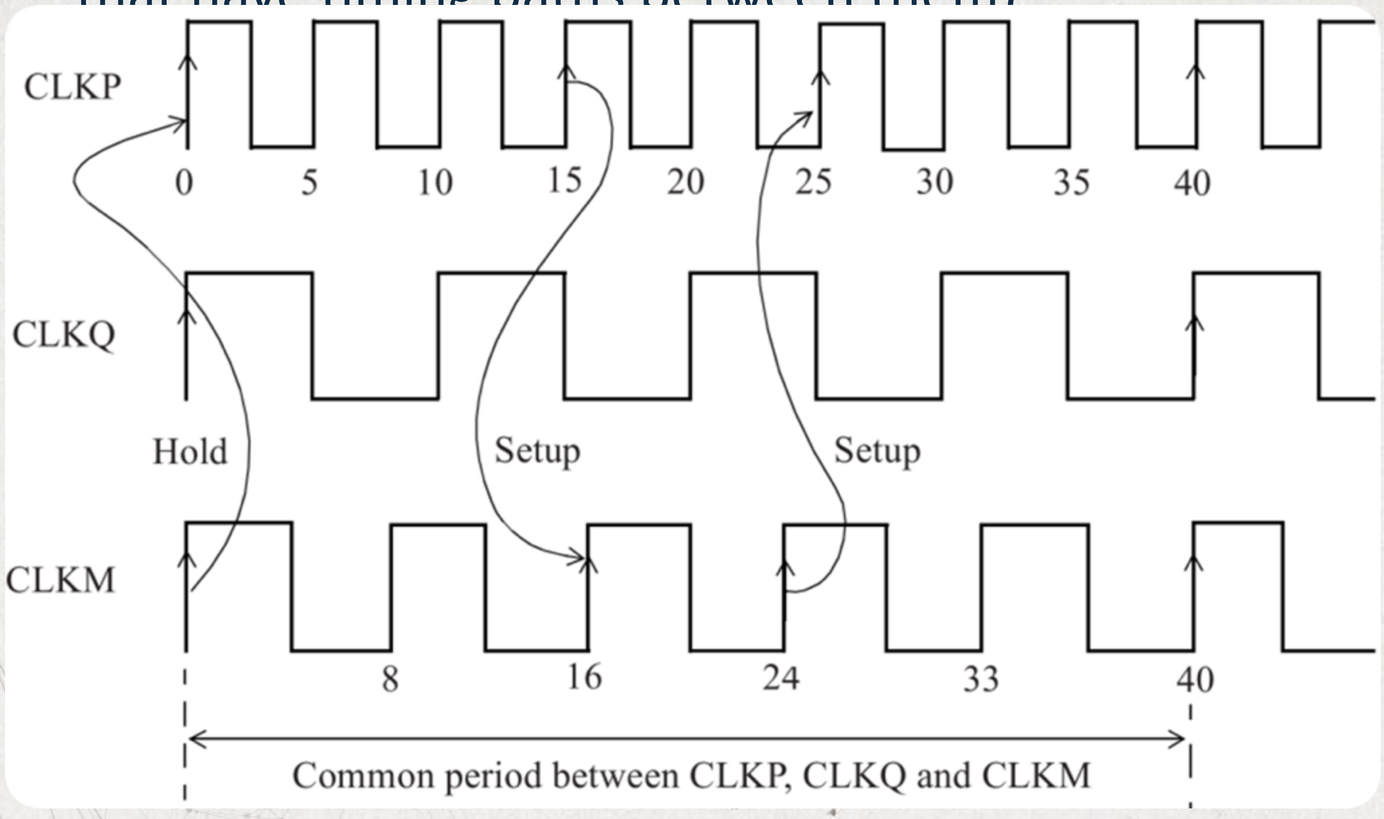



```
create_clock -name CLKM -period 8 -waveform {0 4} [get_ports CLKM]
create_clock -name CLKQ -period 10 -waveform {0 5}
create_clock -name CLKP -period 5 -waveform {0 2.5} [get_ports CLKP]
```

- The setup check occurs over the minimum time between the launch edge and the capture edge of the clock.

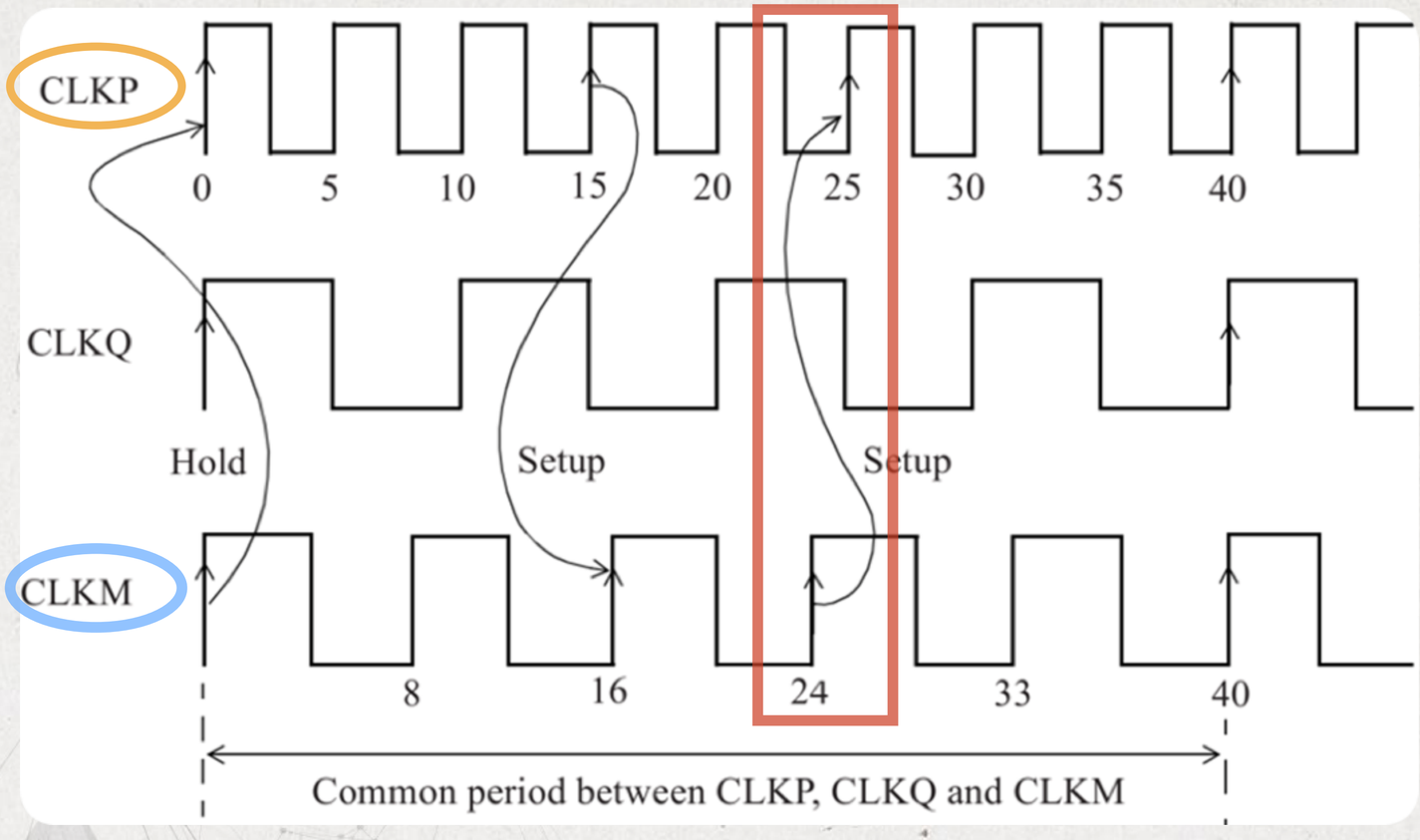


- The timing analysis process computes a common period for the related clocks, and the clocks are then expanded to this base period.
- Note that the common period is found only for related clocks (that is, clocks that have timing paths between them)



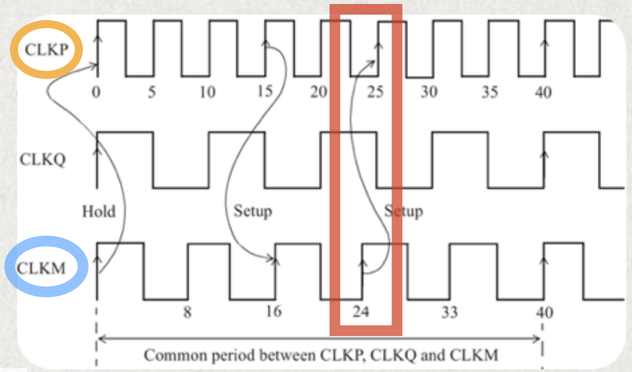
最小公倍数的周期

2- Non-Integer Multiples



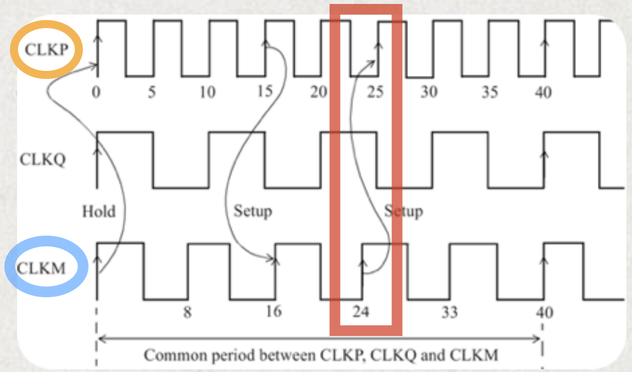

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKM (rise edge)                            24.00      24.00
  clock source latency                               0.00      24.00
  CLKM (in)                                          0.00      24.00 r
  UCKBUF0/C (CKB  )                                  0.06      24.06 r
  UCKBUF1/C (CKB  )                                  0.06      24.11 r
  UFF0/CK (DFF )                                     0.00      24.11 r
  UFF0/Q (DFF ) <-                                   0.14      24.26 f
  UNAND0/ZN (ND2  )                                  0.03      24.29 r
  UFF3/D (DFF )                                      0.00      24.29 r
  data arrival time                                            24.29
```

2- Non-Integer Multiples




```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKM (rise edge)                            24.00      24.00
  clock source latency                               0.00      24.00
  CLKM (in)                                          0.00      24.00 r
  UCKBUF0/C (CKB  )                                  0.06      24.06 r
  UCKBUF1/C (CKB  )                                  0.06      24.11 r
  UFF0/CK (DFF )                                     0.00      24.11 r
  UFF0/Q (DFF ) <-                                   0.14      24.26 f
  UNAND0/ZN (ND2  )                                  0.03      24.29 r
  UFF3/D (DFF )                                      0.00      24.29 r
  data arrival time                                            24.29
```

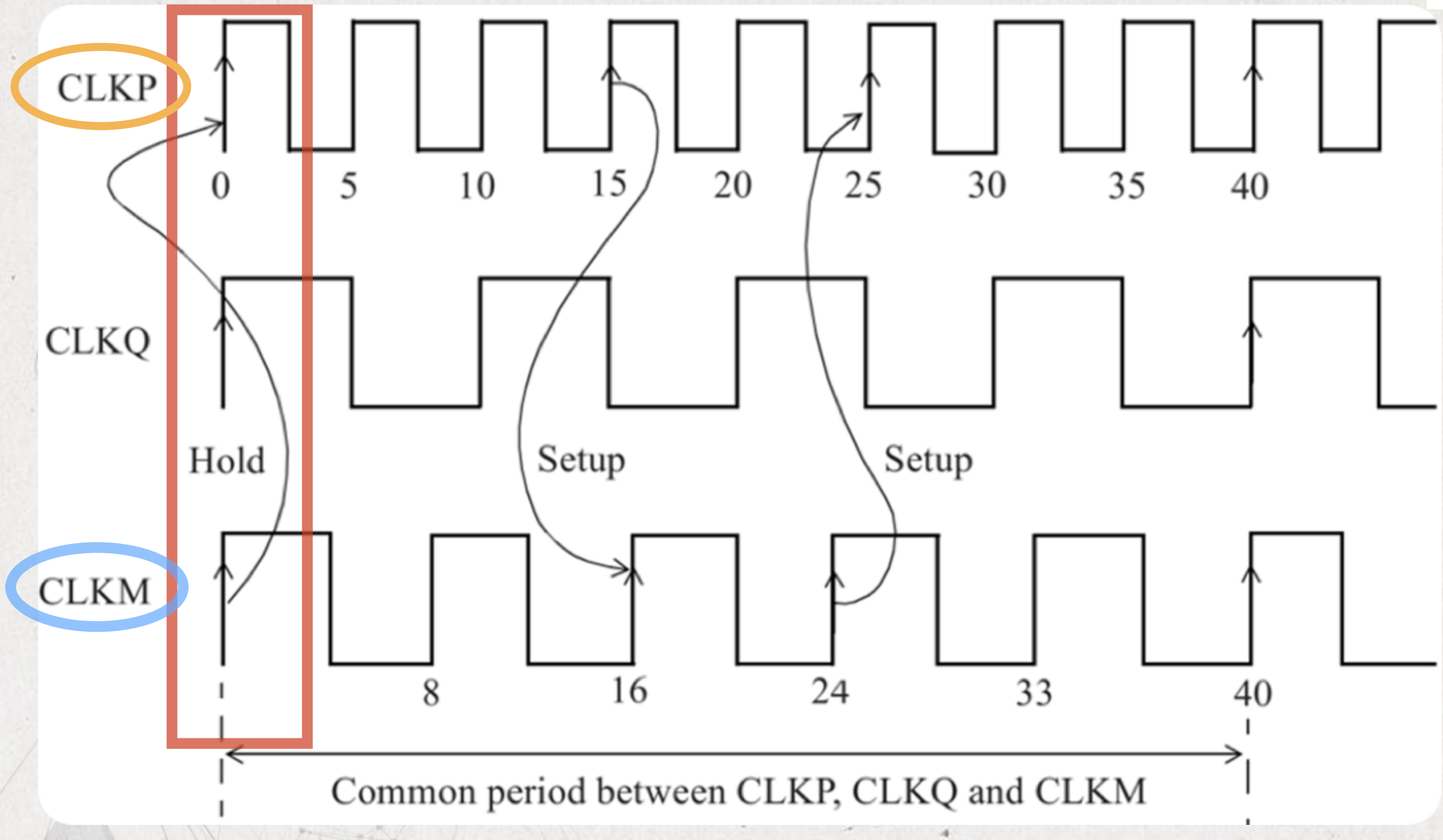
2- Non-Integer Multiples



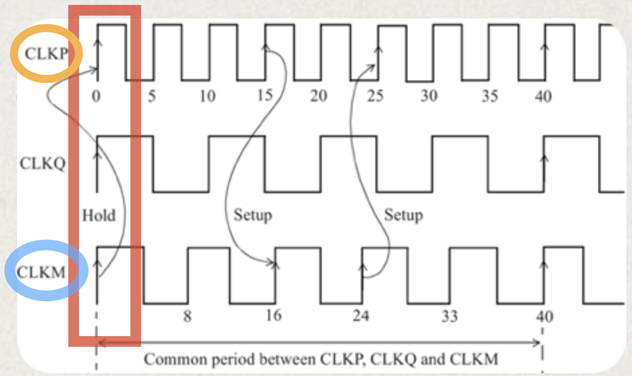
clock CLKP (rise edge)	**25.00**	25.00
clock source latency	0.00	25.00
CLKP (in)	0.00	25.00 r
UCKBUF4/C (CKB)	0.07	25.07 r
UFF3/CK (DFF)	0.00	25.07 r
clock uncertainty	-0.30	24.77
library **setup** time	-0.04	24.72
data required time		24.72
---	---	---
data required time		24.72
data arrival time		-24.29
---	---	---
slack (MET)		0.44

2- Non-Integer Multiples

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: min

  Point                                                   Incr       Path
  ----------------------------------------------------------------------------
  clock CLKM (rise edge)                                  0.00       0.00
  clock source latency                                    0.00       0.00
  CLKM (in)                                               0.00       0.00 r
  UCKBUF0/C (CKB  )                                       0.06       0.06 r
  UCKBUF1/C (CKB  )                                       0.06       0.11 r
  UFF0/CK (DFF )                                          0.00       0.11 r
  UFF0/Q (DFF ) <-                                        0.14       0.26 r
  UNAND0/ZN (ND2  )                                       0.03       0.29 f
  UFF3/D (DFF )                                           0.00       0.29 f
  data arrival time                                                  0.29
```

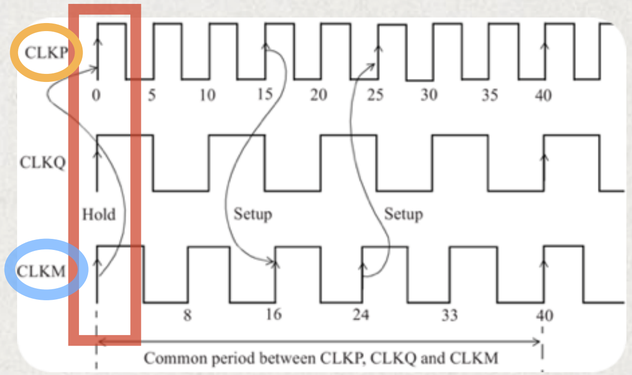


2- Non-Integer Multiples



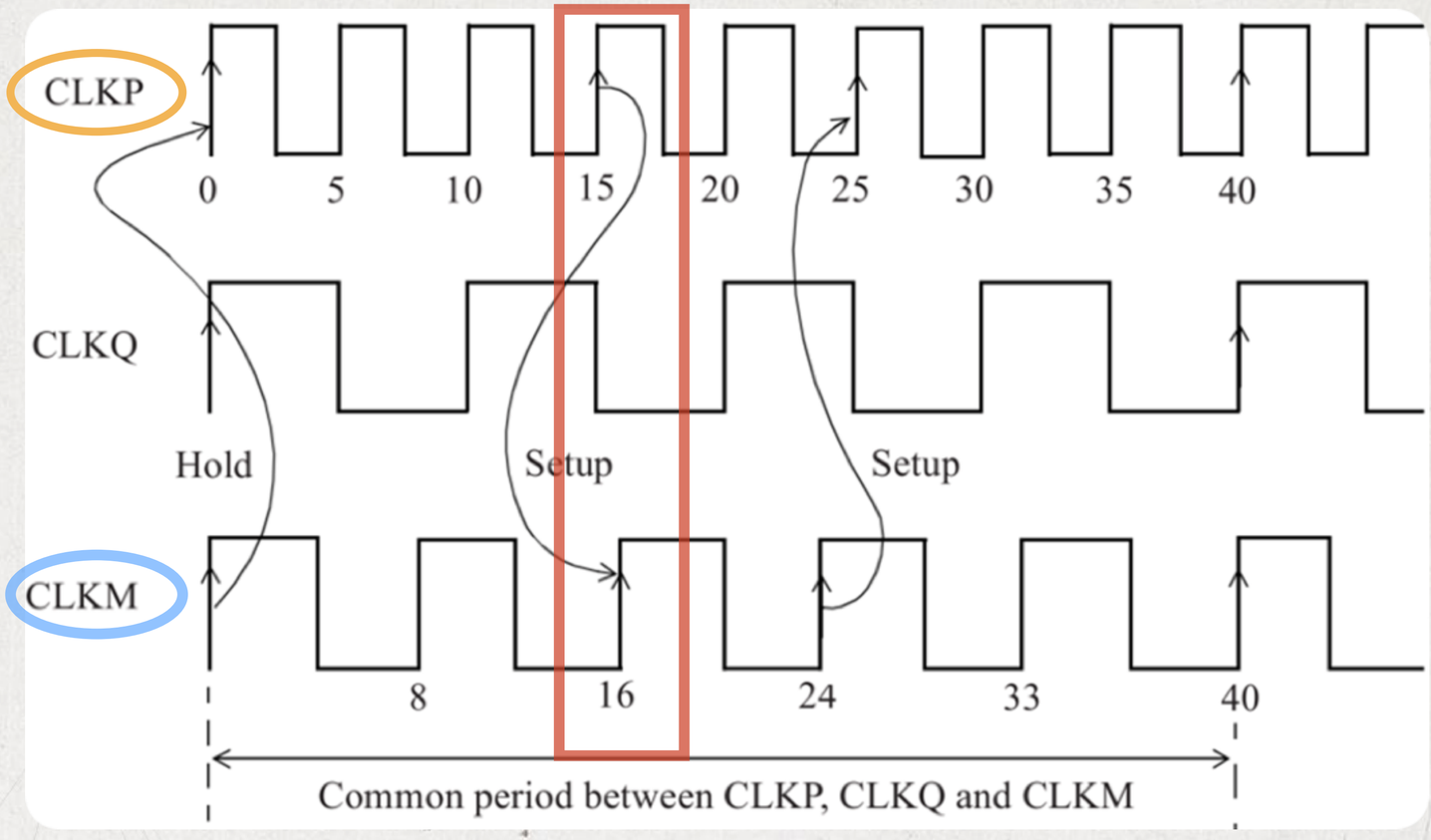

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKM (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKM (in)                                          0.00       0.00 r
  UCKBUF0/C (CKB  )                                  0.06       0.06 r
  UCKBUF1/C (CKB  )                                  0.06       0.11 r
  UFF0/CK (DFF )                                     0.00       0.11 r
  UFF0/Q (DFF ) <-                                   0.14       0.26 r
  UNAND0/ZN (ND2  )                                  0.03       0.29 f
  UFF3/D (DFF )                                      0.00       0.29 f
  data arrival time                                             0.29
```

2- Non-Integer Multiples



clock CLKP (rise edge)	**0.00**	0.00
clock source latency	0.00	0.00
CLKP (in)	0.00	0.00 r
UCKBUF4/C (CKB)	0.07	0.07 r
UFF3/CK (DFF)	0.00	0.07 r
clock uncertainty	0.05	0.12
library **hold** time	0.02	0.13
data required time		0.13
---	---	---
data required time		0.13
data arrival time		-0.29
---	---	---
slack (MET)		0.16

- Now we examine the setup path from the CLKP clock domain to the CLKM clock domain. In this case, the most restrictive setup path is from a launch edge at 15ns of clock CLKP to the capture edge at 16ns of clock CLKM.



2- Non-Integer Multiples

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (rise edge)                            15.00      15.00
  clock source latency                               0.00      15.00
  CLKP (in)                                          0.00      15.00 r
  UCKBUF4/C (CKB  )                                  0.07      15.07 r
  UFF3/CK (DFF )                                     0.00      15.07 r
  UFF3/Q (DFF ) <-                                   0.15      15.22 f
  UNOR0/ZN (NR2  )                                   0.05      15.27 r
  UBUF4/Z (BUFF  )                                   0.05      15.32 r
  UFF1/D (DFF )                                      0.00      15.32 r
  data arrival time                                            15.32
```

clock CLKM (rise edge)	**16.00**	16.00	
clock source latency	0.00	16.00	
CLKM (in)	0.00	16.00	r
UCKBUF0/C (CKB)	0.06	16.06	r
UCKBUF2/C (CKB)	0.07	16.12	r
UFF1/CK (DFF)	0.00	16.12	r
clock uncertainty	-0.30	15.82	
library **setup** time	-0.04	15.78	
data required time		15.78	
data required time		15.78	
data arrival time		-15.32	
slack (MET)		0.46	

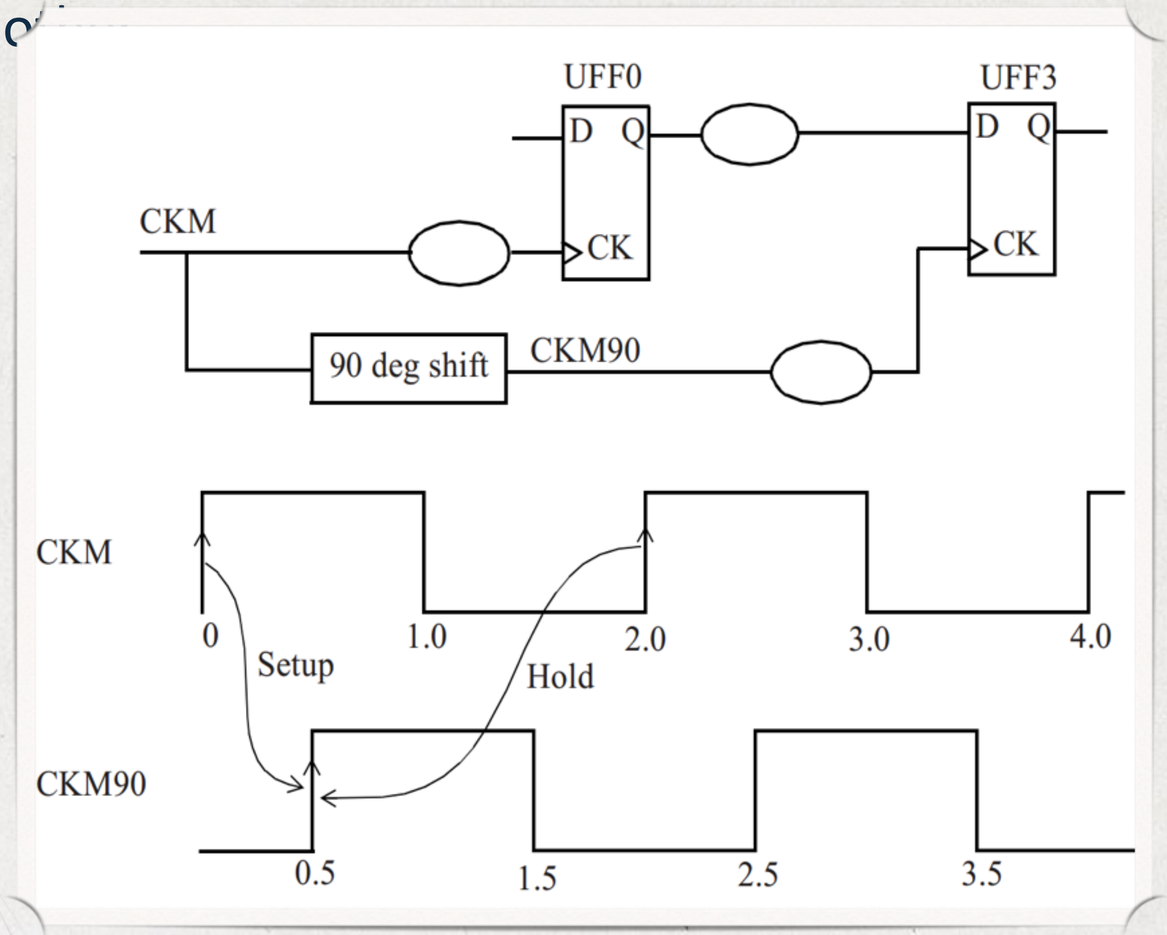
2- Non-Integer Multiples

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKP (in)                                          0.00       0.00 r
  UCKBUF4/C (CKB  )                                  0.07       0.07 r
  UFF3/CK (DFF )                                     0.00       0.07 r
  UFF3/Q (DFF ) <-                                   0.16       0.22 r
  UNOR0/ZN (NR2  )                                   0.02       0.25 f
  UBUF4/Z (BUFF  )                                   0.06       0.30 f
  UFF1/D (DFF )                                      0.00       0.30 f
  data arrival time                                             0.30
```

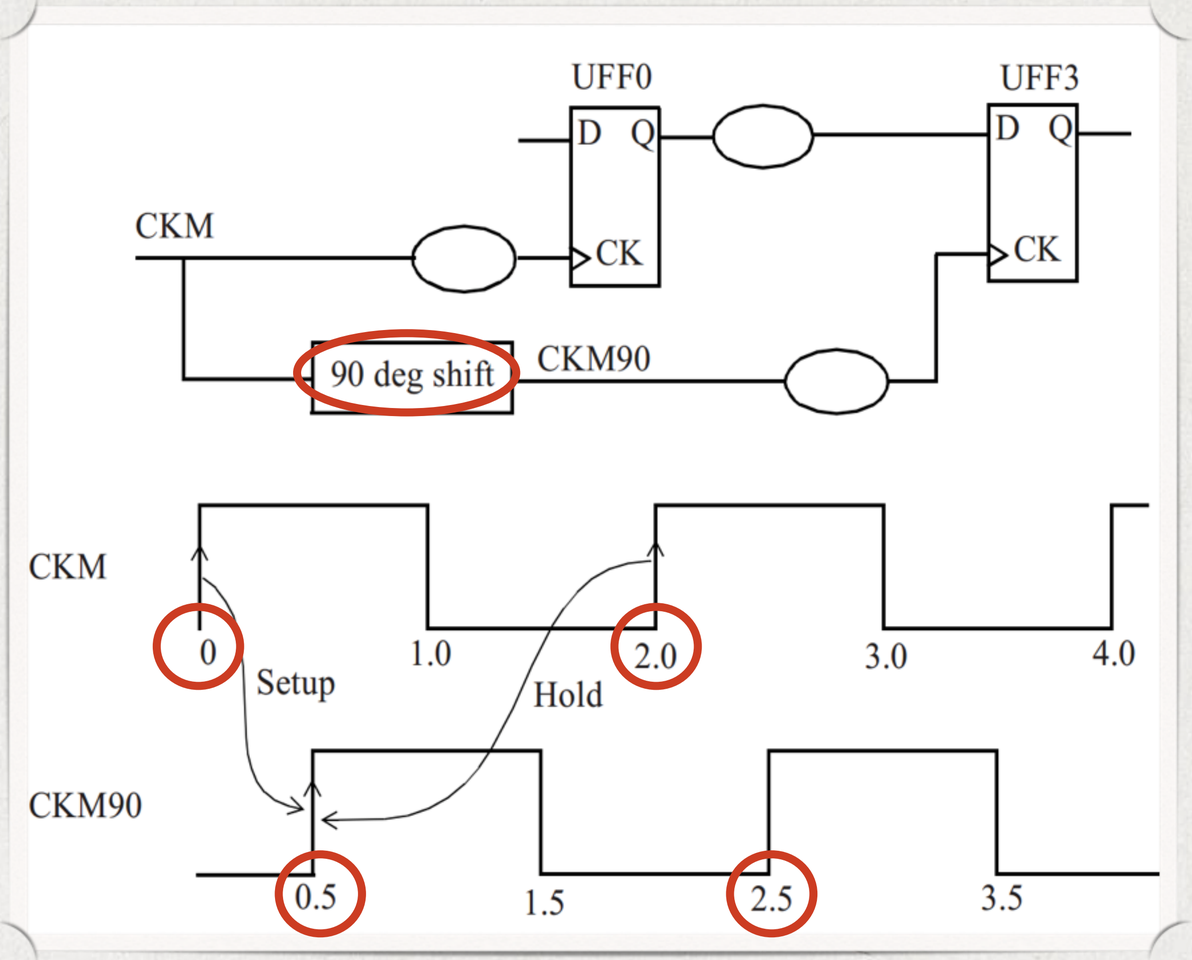
clock CLKM (rise edge)	**0.00**	0.00
clock source latency	0.00	0.00
CLKM (in)	0.00	0.00 r
UCKBUF0/C (CKB)	0.06	0.06 r
UCKBUF2/C (CKB)	0.07	0.12 r
UFF1/CK (DFF)	0.00	0.12 r
clock uncertainty	0.05	0.17
library **hold** time	0.01	0.19
data required time		0.19
---	---	---
data required time		0.19
data arrival time		-0.30
---	---	---
slack (MET)		0.12

3- Phase Shifted

- Here is an example where two clocks are ninety degrees phase-shifted with respect to each o

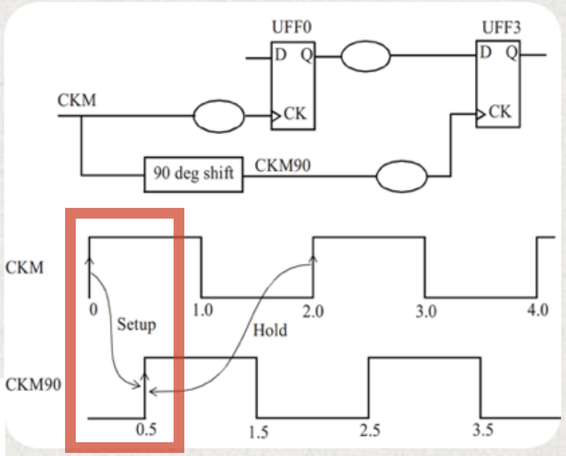


偏移0.5ns



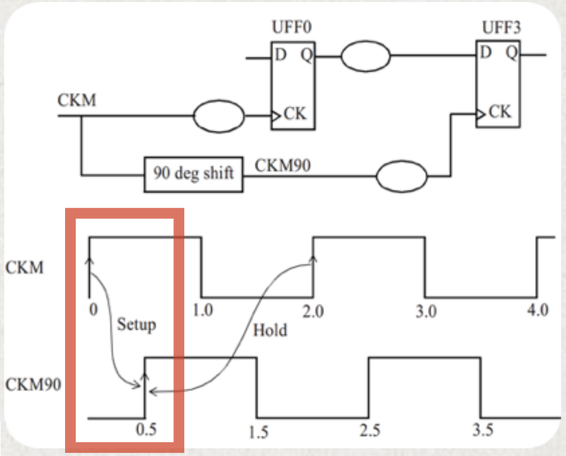

```
create_clock -period 2.0 -waveform {0 1.0} [get_ports CKM]
create_clock -period 2.0 -waveform {0.5 1.5} [get_ports CKM90]
```

3- Phase Shifted



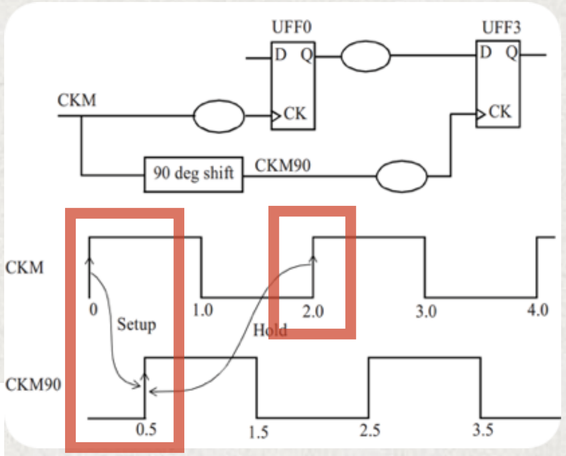

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CKM)
Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CKM90)
  Path Group: CKM90
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------
  clock CKM  (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CKM  (in)                                          0.00       0.00 r
  UCKBUF0/C (CKB  )                                  0.06       0.06 r
  UCKBUF1/C (CKB  )                                  0.06       0.11 r
  UFF0/CK (DF  )                                     0.00       0.11 r
  UFF0/Q (DF  ) <-                                   0.14       0.26 f
  UNAND0/ZN (ND2  )                                  0.03       0.29 r
  UFF3/D (DF  )                                      0.00       0.29 r
  data arrival time                                             0.29
```

3- Phase Shifted



clock CKM90(rise edge)	**0.50**	0.50
clock source latency	0.00	0.50
CKM90(in)	0.00	0.50 r
UCKBUF4/C (CKB)	0.07	0.57 r
UFF3/CK (DF)	0.00	0.57 r
clock uncertainty	-0.30	0.27
library **setup** time	-0.04	0.22
data required time		0.22
data required time		0.22
data arrival time		-0.29
slack (VIOLATED)		-0.06

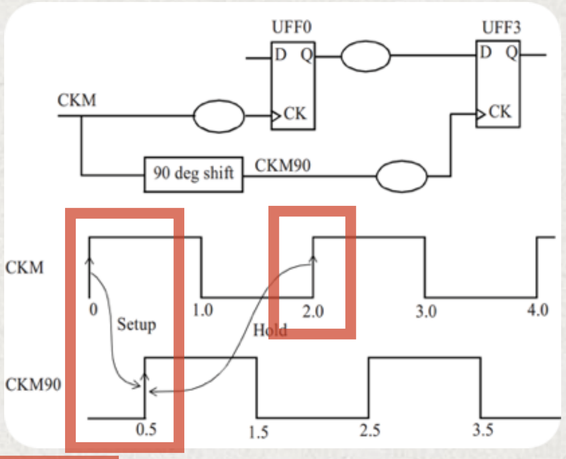
3- Phase Shifted



Startpoint: UFF0 (rising edge-triggered flip-flop clocked by **CKM**)
Endpoint: UFF3 (rising edge-triggered flip-flop clocked by **CKM90**)
  Path Group: **CKM90**
  Path Type: **min**

Point	Incr	Path
clock CKM (rise edge)	**2.00**	2.00
clock source latency	0.00	2.00
CKM (in)	0.00	2.00 r
UCKBUF0/C (CKB)	0.06	2.06 r
UCKBUF1/C (CKB)	0.06	2.11 r
UFF0/CK (DF)	0.00	2.11 r
UFF0/Q (DF) <-	0.14	2.26 r
UNAND0/ZN (ND2)	0.03	2.29 f
UFF3/D (DF)	0.00	2.29 f
data arrival time		2.29

3- Phase Shifted



clock CKM90(rise edge)	**0.50**	0.50	
clock source latency	0.00	0.50	
CLM90(in)	0.00	0.50	r
UCKBUF4/C (CKB)	0.07	0.57	r
UFF3/CK (DF)	0.00	0.57	r
clock uncertainty	0.05	0.62	
library **hold** time	0.02	0.63	
data required time		0.63	
data required time		0.63	
data arrival time		-2.29	
slack (MET)		1.66	

Half-Cycle Paths

- If a design has both negative-edge triggered flip-flops (active clock edge isfalling edge) and positive-edge triggered flip-flops (active clock edge is rising edge), it is likely that half-cycle paths exist in the design. A half-cycle path could be from a rising edge flip-flop to a falling edge flip-flop, or vice versa. Figure 8-19 shows an example when the launch is on the falling edge of the clock of flip-flop UFF5, and the capture is on the rising edge of the clock of flip-flop UFF3.

Half-Cycle Paths

- Figure 8-19 shows an example when the launch is on the falling edge of the clock of flip-flop UFF5, and the capture is on the rising edge of the clock of flip-flop UFF3.

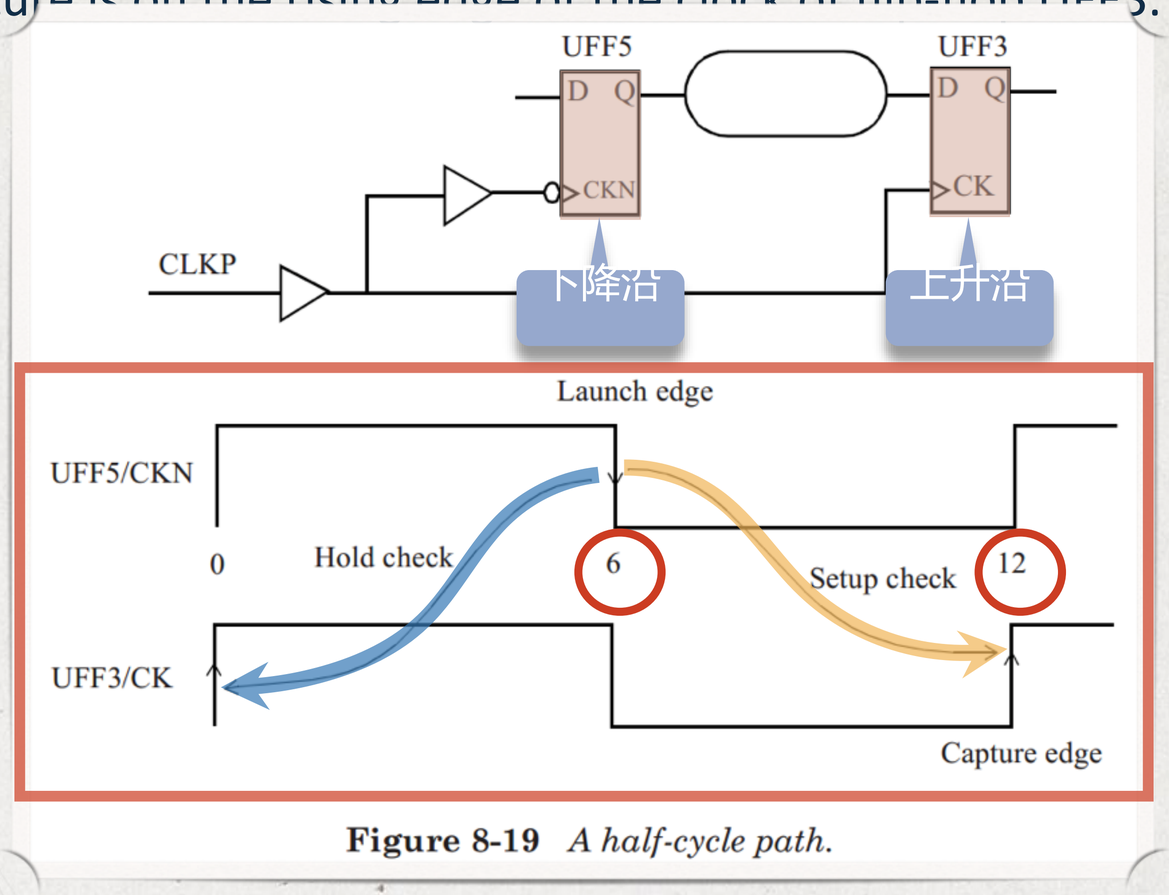


Figure 8-19 *A half-cycle path.*

- Here is the setup timing check path report.

```
Startpoint: UFF5(falling edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------
  clock CLKP (fall edge)                             6.00       6.00
  clock source latency                               0.00       6.00
  CLKP (in)                                          0.00       6.00 f
  UCKBUF4/C (CKB  )                                  0.06       6.06 f
  UCKBUF6/C (CKB  )                                  0.06       6.12 f
  UFF5/CKN (DFN  )                                   0.00       6.12 f
  UFF5/Q (DFN  ) <-                                  0.16       6.28 r
  UNAND0/ZN (ND2  )                                  0.03       6.31 f
  UFF3/D (DFF )                                      0.00       6.31 f
  data arrival time                                             6.31
```

clock CLKP (rise edge)	**12.00**	12.00	
clock source latency	0.00	12.00	
CLKP (in)	0.00	12.00	**r**
UCKBUF4/C (CKB)	0.07	12.07	r
UFF3/CK (DFF)	0.00	12.07	r
clock uncertainty	-0.30	11.77	
library **setup** time	-0.03	11.74	
data required time		11.74	
data required time		11.74	
data arrival time		-6.31	
slack (MET)		5.43	

- Note the edge specification in the Startpoint and Endpoint. The falling edge occurs at 6ns and the rising edge occurs at 12ns. Thus, the data gets only a half-cycle, which is 6ns, to propagate to the capture flip-flop.

Half-Cycle Paths

```
Startpoint: UFF5(falling edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (fall edge)                             6.00       6.00
  clock source latency                               0.00       6.00
  CLKP (in)                                          0.00       6.00 f
  UCKBUF4/C (CKB  )                                  0.06       6.06 f
  UCKBUF6/C (CKB  )                                  0.06       6.12 f
  UFF5/CKN (DFN  )                                   0.00       6.12 f
  UFF5/Q (DFN  ) <-                                  0.16       6.28 r
  UNAND0/ZN (ND2  )                                  0.03       6.31 f
  UFF3/D (DFF )                                      0.00       6.31 f
  data arrival time                                             6.31
```

clock CLKP (rise edge)	**0.00**	0.00
clock source latency	0.00	0.00
CLKP (in)	0.00	0.00 r
UCKBUF4/C (CKB)	0.07	0.07 r
UFF3/CK (DFF)	0.00	0.07 r
clock uncertainty	0.05	0.12
library **hold** time	0.02	0.13
data required time		0.13
data required time		0.13
data arrival time		-6.31
slack (MET)		6.18

- The hold check always occurs one cycle prior to the capture edge. Since the capture edge occurs at 12ns, the previous capture edge is at 0ns, and hence the hold gets checked at 0ns. This effectively adds a half-cycle margin for hold checking and thus results in a large positive slack on hold.

False Paths

- It is possible that certain timing paths are not real (or not possible) in the actual functional operation of the design. Such paths can be turned off during STA by setting these as false paths. A false path is ignored by the STA for analysis.

False Paths

- from one clock domain to another clock domain;
- from a clock pin of a flip-flop to the input of another flip-flop;
- through a pin of a cell;
- or a combination of these.

False Paths

- When a false path is specified through a pin of a cell, all paths that go through that pin are ignored for timing analysis. The advantage of identifying the false paths is that the analysis space is reduced, thereby allowing the analysis to focus only on the real paths. This helps cut down the analysis time as well. However, too many false paths which are wildcarded using the through specification can slow down the analysis.

Half-Cycle Paths

- A false path is set using the set_false_path specification. Here are some examples.

```
set_false_path -from [get_clocks CLK] \-to [get_clocks CORE_CLK]
```

- Any path starting from the SCAN_CLK domain to the CORE_CLK domain is a false path.

```
set_false_path -through [get_pins UMUXO/S]
```

- Any path going through this pin is false.

Half-Cycle Paths

- A false path is set using the set_false_path specification. Here are some examples

```
set_false_path \-through [get_pins SAD_CORE/RSTN]
```

- The false path specifications can also be specified to, through, or from a module pin instance.

```
set_false_path -to [get_ports TEST_REG*]
```

- All paths that end in port named TEST_REG* are false paths.

```
set_false_path -through UINV/Z-through UAND0/Z
```

- Any path that goes through both of these pins in this order is false.

Half-Cycle Paths

- Few recommendations on setting false paths are given below. To set a false path between two clock domains, use:

```
set_false_path -from [get_clocks clockA] \-to [get_clocks clockB]
```

- instead of:

```
set_false_path -from [get_pins {regA_*} /CP] \-to [get_pins {regB_*} /D]
```

The second form is much slower

False Paths

- Another recommendation is to minimize the usage of -through options, as it adds unnecessary runtime complexity. The -through option should only be used where it is absolutely necessary and there is no alternate way to specify the false path.

False Paths

- From an optimization perspective, another guideline is to not use a false path when a multicycle path is the real intent. If a signal is sampled at a known or predictable time, no matter how far out, a multicycle path specification should be used so that the path has some constraint and gets optimized to meet the multicycle constraint. If a false path is used on a path that is sampled many clock cycles later, optimization of the remaining logic may invariably slow this path even beyond what may be necessary.