数字集成电路静态时序分析基础

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Part 5: Timing Verification

CONTENT

1. Timing across Clock Domains
2. Multiple Clocks

Timing across Clock Domains

1 Slow to Fast Clock Domains

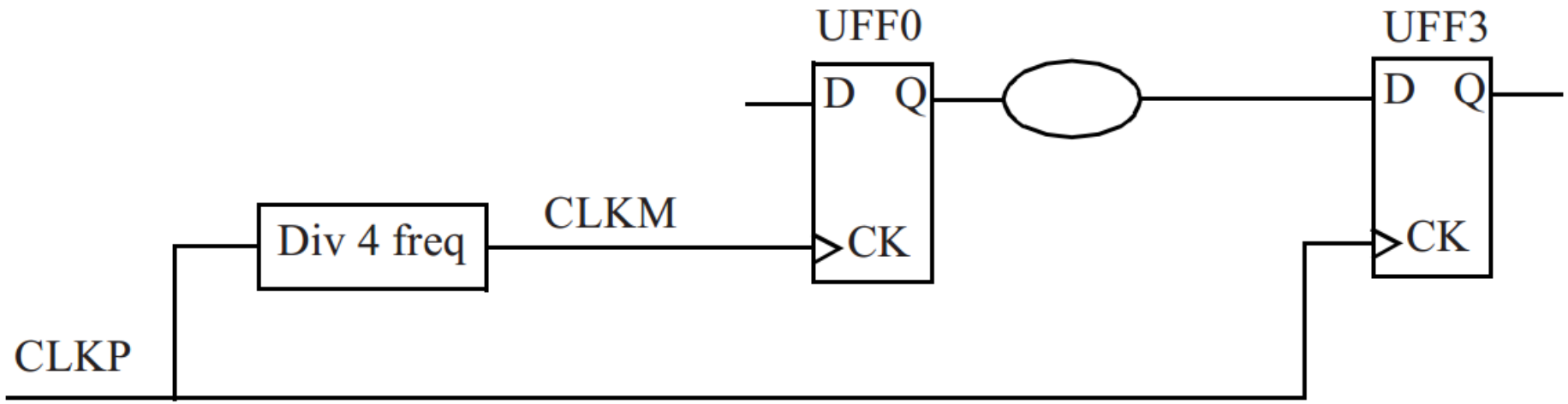


Figure 8-22 *Path from a slow clock to a faster clock.*

1 Slow to Fast Clock Domains

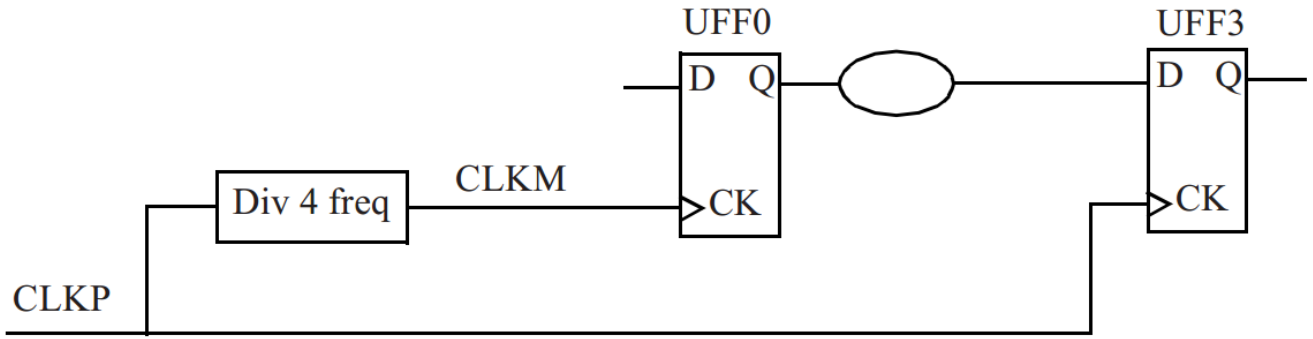


Figure 8-22 *Path from a slow clock to a faster clock.*

Here are the clock definitions for our example.

```
create_clock -name CLKM \
  -period 20 -waveform {0 10} [get_ports CLKM]
create_clock -name CLKP \
  -period 5 -waveform {0 2.5} [get_ports CLKP]
```

1 Slow to Fast Clock Domains

By default, the most constraining setup edge relationship is used, which in this case is the very next capture edge. Here is a setup path report that shows this.

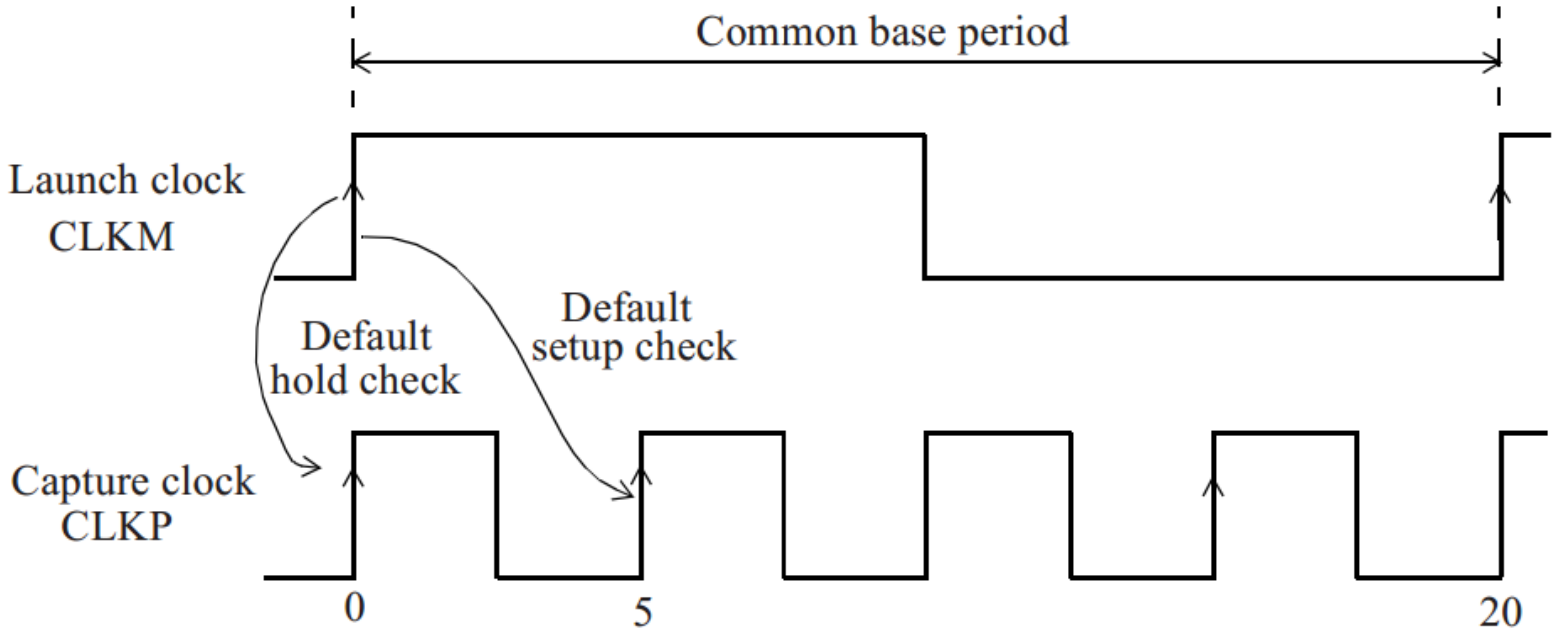


Figure 8-23 *Setup and hold checks with slow to fast path.*

Timing across Clock Domains

1 Slow to Fast Clock Domains

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------
  clock CLKM (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKM (in)                                          0.00       0.00 r
  UCKBUF0/C (CKB  )                                  0.06       0.06 r
  UCKBUF1/C (CKB  )                                  0.06       0.11 r
  UFF0/CK (DFF )                                     0.00       0.11 r
  UFF0/Q (DFF ) <-                                   0.14       0.26 f
  UNAND0/ZN (ND2  )                                  0.03       0.29 r
  UFF3/D (DFF )                                      0.00       0.29 r
  data arrival time                                             0.29
```

Timing across Clock Domains

1 Slow to Fast Clock Domains

```
clock CLKP (rise edge)                          5.00        5.00
clock source latency                            0.00        5.00
CLKP (in)                                       0.00        5.00 r
UCKBUF4/C (CKB  )                               0.07        5.07 r
UFF3/CK (DFF )                                  0.00        5.07 r
clock uncertainty                              -0.30        4.77
library setup time                             -0.04        4.72
data required time                                          4.72
-----------------------------------------------------------------
data required time                                          4.72
data arrival time                                          -0.29
-----------------------------------------------------------------
slack (MET)                                                 4.44
```

Notice that the launch clock is at time 0ns while the capture clock is at time 5ns.

Timing across Clock Domains

1 Slow to Fast Clock Domains

As discussed earlier, hold checks are related to the setup checks and ensure that the data launched by a clock edge does not interfere with the previous capture. Here is the hold check timing report.

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------
  clock CLKM (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKM (in)                                          0.00       0.00 r
  UCKBUF0/C (CKB  )                                  0.06       0.06 r
  UCKBUF1/C (CKB  )                                  0.06       0.11 r
  UFF0/CK (DFF )                                     0.00       0.11 r
  UFF0/Q (DFF ) <-                                   0.14       0.26 r
  UNAND0/ZN (ND2  )                                  0.03       0.29 f
  UFF3/D (DFF )                                      0.00       0.29 f
  data arrival time                                             0.29
```

Timing across Clock Domains

1 Slow to Fast Clock Domains

In the above example, we can see that the launch data is available every fourth cycle of the capture clock. Let us assume that the intention is not to capture data on the very next active edge of CLKP, but to capture on every 4th capture edge. This assumption gives the combinational logic between the flip-flops four periods of CLKP to propagate, which is 20ns. We can do this by setting the following multicycle specification:

```
set_multicycle_path 4 -setup \
  -from [get_clocks CLKM] -to [get_clocks CLKP] -end
```

Timing across Clock Domains

1 Slow to Fast Clock Domains

The -end specifies that the multicycle of 4 refers to the end point or the capture clock. This multicycle specification changes the setup and hold checks to the ones shown in Figure 8-24.

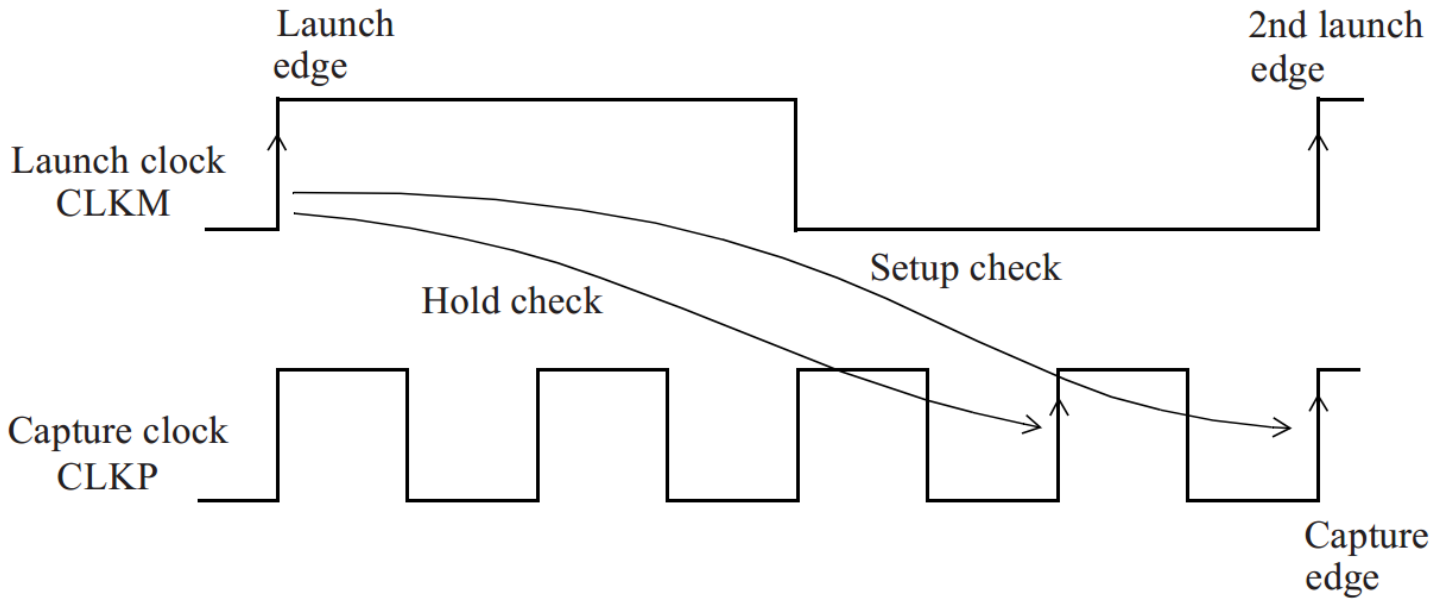


Figure 8-24 *Multicycle of 4 between clock domains.*

Timing across Clock Domains

1 Slow to Fast Clock Domains

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLKM (rise edge)                   0.00       0.00
  clock source latency                     0.00       0.00
  CLKM (in)                                0.00       0.00 r
  UCKBUF0/C (CKB  )                        0.06       0.06 r
  UCKBUF1/C (CKB  )                        0.06       0.11 r
  UFF0/CK (DFF )                           0.00       0.11 r
  UFF0/Q (DFF ) <-                         0.14       0.26 f
  UNAND0/ZN (ND2  )                        0.03       0.29 r
  UFF3/D (DFF )                            0.00       0.29 r
  data arrival time                                   0.29
```

Timing across Clock Domains

1 Slow to Fast Clock Domains

```
clock CLKP (rise edge)                          20.00       20.00
clock source latency                             0.00       20.00
CLKP (in)                                        0.00       20.00 r
UCKBUF4/C (CKB  )                                0.07       20.07 r
UFF3/CK (DFF )                                   0.00       20.07 r
clock uncertainty                               -0.30       19.77
library setup time                              -0.04       19.72
data required time                                          19.72
-----------------------------------------------------------------
data required time                                          19.72
data arrival time                                           -0.29
-----------------------------------------------------------------
slack (MET)                                                 19.44
```

Timing across Clock Domains

1 Slow to Fast Clock Domains

Figure 8-24 shows the hold check - note that the hold check is derived from the setup check and defaults to one cycle preceding the intended capture edge.

Here is the hold timing report. Notice that the hold capture edge is at **15ns**, one cycle prior to the setup capture edge.

Timing across Clock Domains

1 Slow to Fast Clock Domains

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: min

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLKM (rise edge)                   0.00       0.00
  clock source latency                     0.00       0.00
  CLKM (in)                                0.00       0.00 r
  UCKBUF0/C (CKB  )                        0.06       0.06 r
  UCKBUF1/C (CKB  )                        0.06       0.11 r
  UFF0/CK (DFF )                           0.00       0.11 r
  UFF0/Q (DFF ) <-                         0.14       0.26 r
  UNAND0/ZN (ND2  )                        0.03       0.29 f
  UFF3/D (DFF )                            0.00       0.29 f
  data arrival time                                   0.29
```

Timing across Clock Domains

1 Slow to Fast Clock Domains

```
clock CLKP (rise edge)                    15.00       15.00
clock source latency                       0.00       15.00
CLKP (in)                                  0.00       15.00 r
UCKBUF4/C (CKB  )                          0.07       15.07 r
UFF3/CK (DFF )                             0.00       15.07 r
clock uncertainty                          0.05       15.12
library hold time                          0.02       15.13
data required time                                    15.13
-------------------------------------------------------------
data required time                                    15.13
data arrival time                                     -0.29
-------------------------------------------------------------
slack (VIOLATED)                                     -14.84
```

Timing across Clock Domains

1 Slow to Fast Clock Domains

In most designs, this is not the intended check, and the hold check should be moved all the way back to where the launch edge is. We do this by setting a hold multicycle specification of 3.

```
set_multicycle_path 3 -hold \
  -from [get_clocks CLKM] -to [get_clocks CLKP] -end
```

The cycle of 3 moves the hold checking edge back three cycles, that is, to time 0ns.

The distinction with a setup multicycle is that in setup, the setup capture edge moves forward by the specified number of cycles from the default setup capture edge; in a hold multicycle, the hold check edge moves backward from the default hold check edge (one cycle before setup edge).

1 Slow to Fast Clock Domains

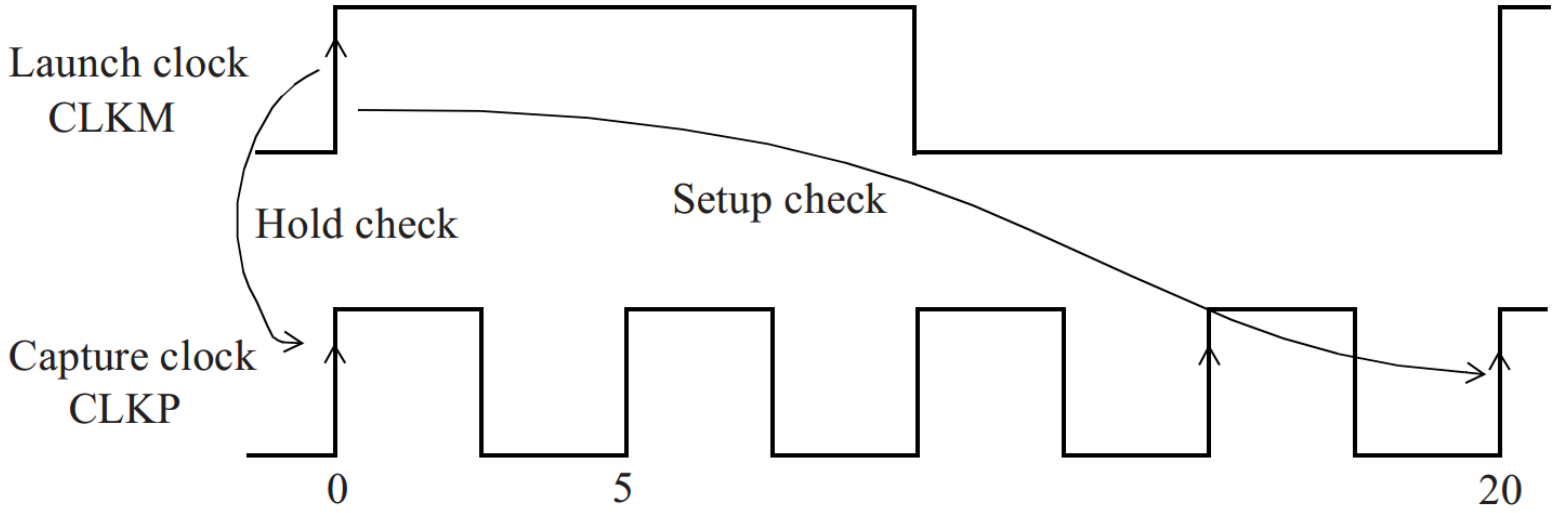


Figure 8-25 *Hold time relaxed with multicycle hold specification.*

Timing across Clock Domains

1 Slow to Fast Clock Domains

In summary, if a setup multicycle of **N cycles** is specified, then most likely a hold multicycle of **N-1 cycles** should also be specified.

2 Fast to Slow Clock Domains

In this subsection, we consider examples where the data path goes from a fast clock domain to a slow clock domain. The default setup and hold checks are as shown in Figure 8-26 when the following clock definitions are used.

```
create_clock -name CLKM \
  -period 20 -waveform {0 10} [get_ports CLKM]
create_clock -name CLKP \
  -period 5 -waveform {0 2.5} [get_ports CLKP]
```

Timing across Clock Domains

2 Fast to Slow Clock Domains

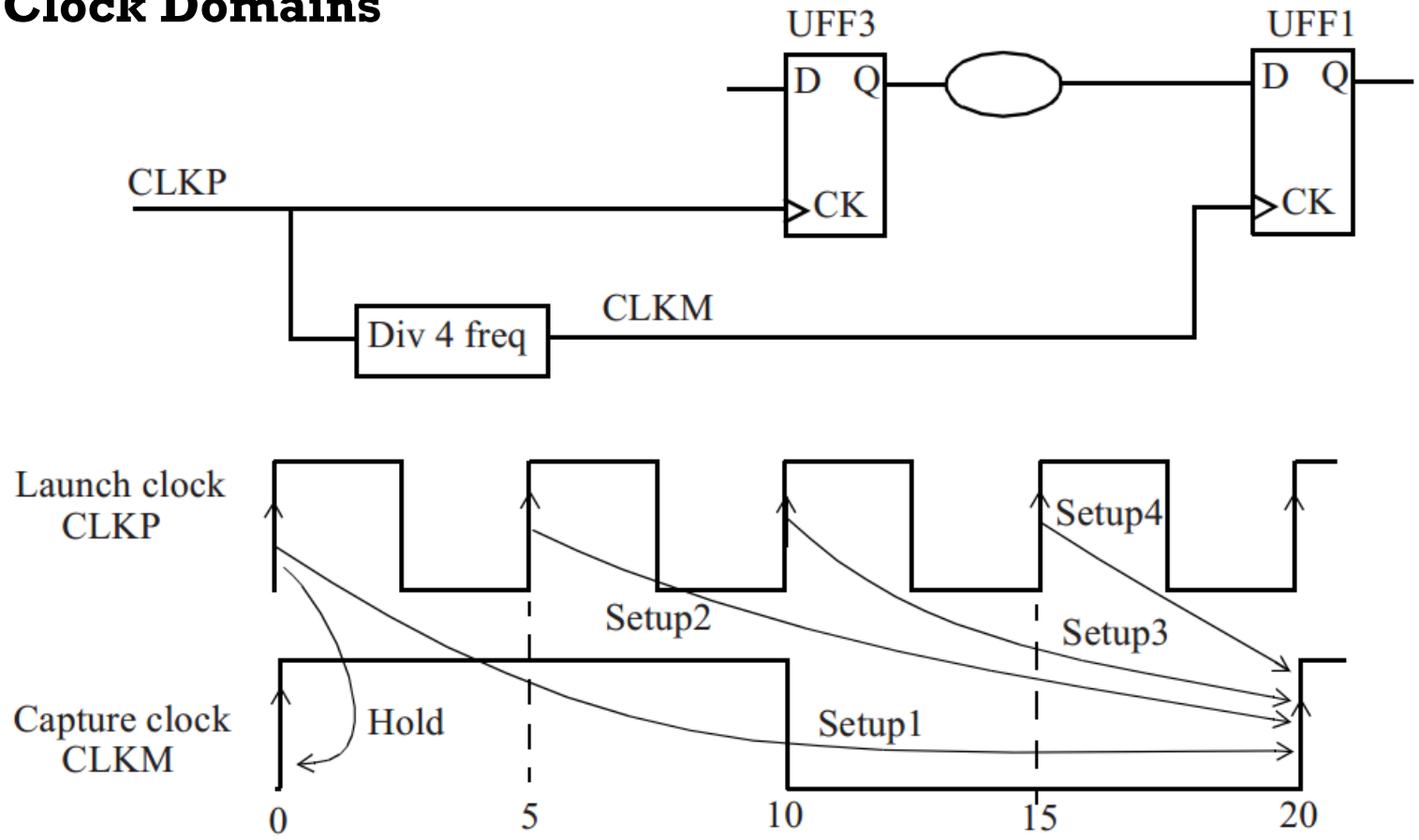


Figure 8-26 *Path from fast clock to slow clock domain.*

2 Fast to Slow Clock Domains

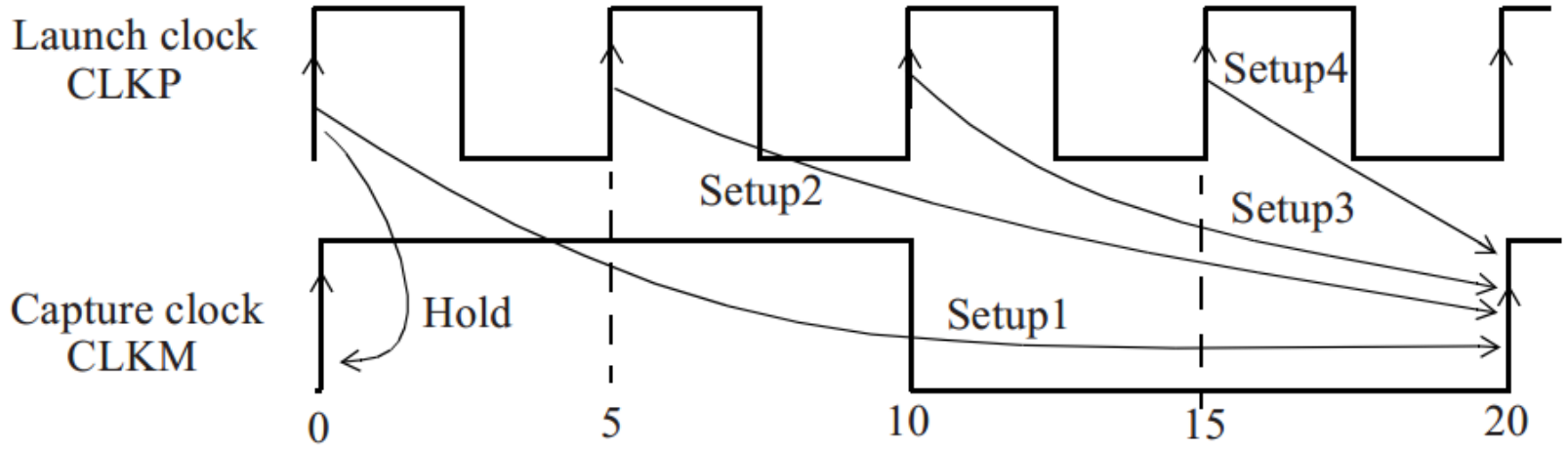


Figure 8-26 *Path from fast clock to slow clock domain.*

There are four setup timing checks possible; see Setup1, Setup2, Setup3 and Setup4 in the figure. However, the most restrictive one is the Setup4 check. Here is the path report of this most restrictive path. Notice that the launch clock edge is at 15ns and the capture clock edge is at 20ns.

Timing across Clock Domains

2 Fast to Slow Clock Domains

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (rise edge)                            15.00      15.00
  clock source latency                               0.00      15.00
  CLKP (in)                                          0.00      15.00 r
  UCKBUF4/C (CKB  )                                  0.07      15.07 r
  UFF3/CK (DFF )                                     0.00      15.07 r

  UFF3/Q (DFF ) <-                                   0.15      15.22 f
  UNOR0/ZN (NR2  )                                   0.05      15.27 r
  UBUF4/Z (BUFF  )                                   0.05      15.32 r
  UFF1/D (DFF )                                      0.00      15.32 r
  data arrival time                                            15.32
```

Timing across Clock Domains

2 Fast to Slow Clock Domains

```
clock CLKM (rise edge)                          20.00       20.00
clock source latency                             0.00       20.00
CLKM (in)                                        0.00       20.00 r
UCKBUF0/C (CKB  )                                0.06       20.06 r
UCKBUF2/C (CKB  )                                0.07       20.12 r
UFF1/CK (DFF )                                   0.00       20.12 r
clock uncertainty                               -0.30       19.82
library setup time                              -0.04       19.78
data required time                                          19.78
-------------------------------------------------------------------
data required time                                          19.78
data arrival time                                          -15.32
-------------------------------------------------------------------
slack (MET)                                                 4.46
```

2 Fast to Slow Clock Domains

Similar to the setup checks, there are four hold checks possible.

Figure 8-26 shows the most restrictive hold check which ensures that the capture edge at 0ns does not capture the data being launched at 0ns.

Here is the timing report for this hold check.

Timing across Clock Domains

2 Fast to Slow Clock Domains

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKP (in)                                          0.00       0.00 r
  UCKBUF4/C (CKB  )                                  0.07       0.07 r
  UFF3/CK (DFF )                                     0.00       0.07 r
  UFF3/Q (DFF ) <-                                   0.16       0.22 r
  UNOR0/ZN (NR2  )                                   0.02       0.25 f
  UBUF4/Z (BUFF  )                                   0.06       0.30 f
  UFF1/D (DFF )                                      0.00       0.30 f
  data arrival time                                             0.30
```

Timing across Clock Domains

2 Fast to Slow Clock Domains

```
clock CLKM (rise edge)                          0.00          0.00
clock source latency                            0.00          0.00
CLKM (in)                                       0.00          0.00 r
UCKBUF0/C (CKB  )                               0.06          0.06 r
UCKBUF2/C (CKB  )                               0.07          0.12 r
UFF1/CK (DFF )                                  0.00          0.12 r
clock uncertainty                               0.05          0.17
library hold time                               0.01          0.19
data required time                                            0.19
-------------------------------------------------------------------
data required time                                            0.19
data arrival time                                            -0.30
-------------------------------------------------------------------
slack (MET)                                                   0.12
```

Timing across Clock Domains

2 Fast to Slow Clock Domains

In general, a designer may specify the data path from the fast clock to the slow clock to be a multicycle path. If the setup check is relaxed to provide two cycles of the faster clock for the data path, the following is included for this multicycle specification:

```
set_multicycle_path 2 -setup \
  -from [get_clocks CLKP] -to [get_clocks CLKM] -start

set_multicycle_path 1 -hold \
  -from [get_clocks CLKP] -to [get_clocks CLKM] -start
# The -start option refers to the launch clock and is
# the default for a multicycle hold.
```

2 Fast to Slow Clock Domains

In this case, Figure 8-27 shows the clock edges used for the setup and hold checks. The -start option specifies that the unit for the number of cycles (2 in this case) is that of the launch clock (CLKP in this case). The setup multicycle of 2 moves the launch edge one edge prior to the default launch edge, that is, at 10ns instead of the default 15ns. The hold multicycle ensures that the capture of the earlier data can reliably occur at 0ns due to the launch edge also at 0ns.

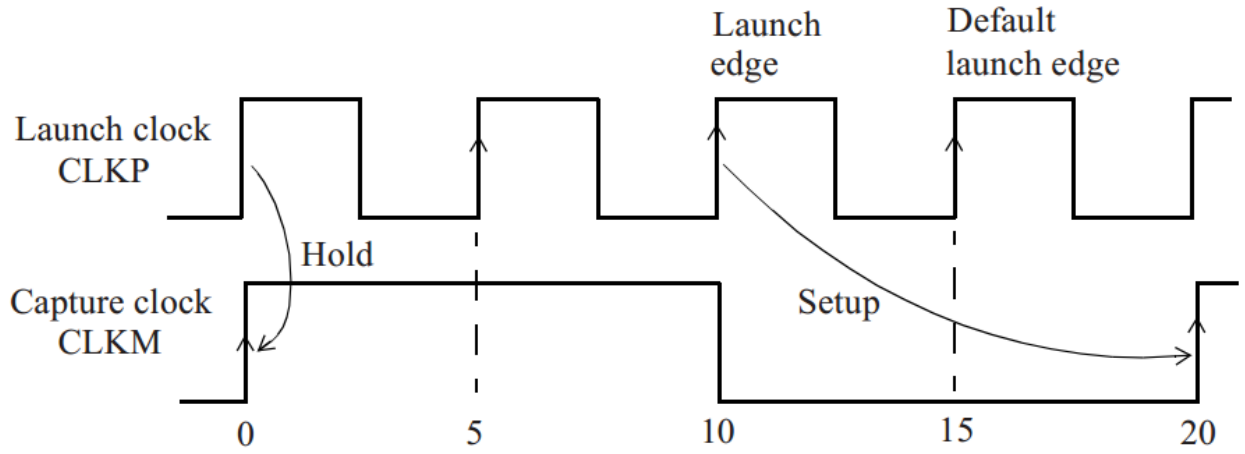


Figure 8-27 *Setup multicycle of 2.*

Timing across Clock Domains

2 Fast to Slow Clock Domains

Here is the setup path report. As expected, the launch clock edge is at 10ns and the capture clock edge is at 20ns.

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: max

  Point                                          Incr       Path
  -----------------------------------------------------------------
  clock CLKP (rise edge)                        10.00      10.00
  clock source latency                           0.00      10.00
  CLKP (in)                                      0.00      10.00 r
  UCKBUF4/C (CKB  )                              0.07      10.07 r
  UFF3/CK (DFF )                                 0.00      10.07 r
  UFF3/Q (DFF ) <-                               0.15      10.22 f
  UNOR0/ZN (NR2  )                               0.05      10.27 r
  UBUF4/Z (BUFF  )                               0.05      10.32 r
  UFF1/D (DFF )                                  0.00      10.32 r
  data arrival time                                        10.32
```

Timing across Clock Domains

2 Fast to Slow Clock Domains

Here is the setup path report. As expected, the launch clock edge is at 10ns and the capture clock edge is at 20ns.

```
clock CLKM (rise edge)                    20.00      20.00
clock source latency                       0.00      20.00
CLKM (in)                                  0.00      20.00 r
UCKBUF0/C (CKB  )                          0.06      20.06 r
UCKBUF2/C (CKB  )                          0.07      20.12 r
UFF1/CK (DFF )                             0.00      20.12 r
clock uncertainty                         -0.30      19.82
library setup time                        -0.04      19.78
data required time                                   19.78
-------------------------------------------------------------
data required time                                   19.78
data arrival time                                   -10.32
-------------------------------------------------------------
slack (MET)                                          9.46
```

Timing across Clock Domains

2 Fast to Slow Clock Domains

Here is the hold path timing report. The hold check is at 0ns where both the capture and launch clocks have rising edges.

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------
  clock CLKP (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKP (in)                                          0.00       0.00 r
  UCKBUF4/C (CKB  )                                  0.07       0.07 r
  UFF3/CK (DFF )                                     0.00       0.07 r
  UFF3/Q (DFF ) <-                                   0.16       0.22 r
  UNOR0/ZN (NR2  )                                   0.02       0.25 f
  UBUF4/Z (BUFF  )                                   0.06       0.30 f
  UFF1/D (DFF )                                      0.00       0.30 f
  data arrival time                                             0.30
```

Timing across Clock Domains

2 Fast to Slow Clock Domains

Here is the hold path timing report. The hold check is at 0ns where both the capture and launch clocks have rising edges.

```
clock CLKM (rise edge)                          0.00       0.00
clock source latency                            0.00       0.00
CLKM (in)                                       0.00       0.00 r
UCKBUF0/C (CKB  )                               0.06       0.06 r
UCKBUF2/C (CKB  )                               0.07       0.12 r
UFF1/CK (DFF )                                  0.00       0.12 r
clock uncertainty                               0.05       0.17
library hold time                               0.01       0.19
data required time                                         0.19
-------------------------------------------------------------------
data required time                                         0.19
data arrival time                                         -0.30
-------------------------------------------------------------------
slack (MET)                                                0.12
```

Timing across Clock Domains

2 Fast to Slow Clock Domains

Unlike the case of paths from slow to fast clock domains, a good rule of thumb for multi-frequency multicycle path specification in the case of paths from fast to slow clock domains is to use the -start option. The setup and hold checks are then adjusted based upon the fast clock.

Part 5: Timing Verification

CONTENT

1. Timing across Clock Domains
2. Multiple Clocks

1- Integer Multiples

Often there are multiple clocks defined in a design with frequencies that are simple (or integer) multiples of each other.

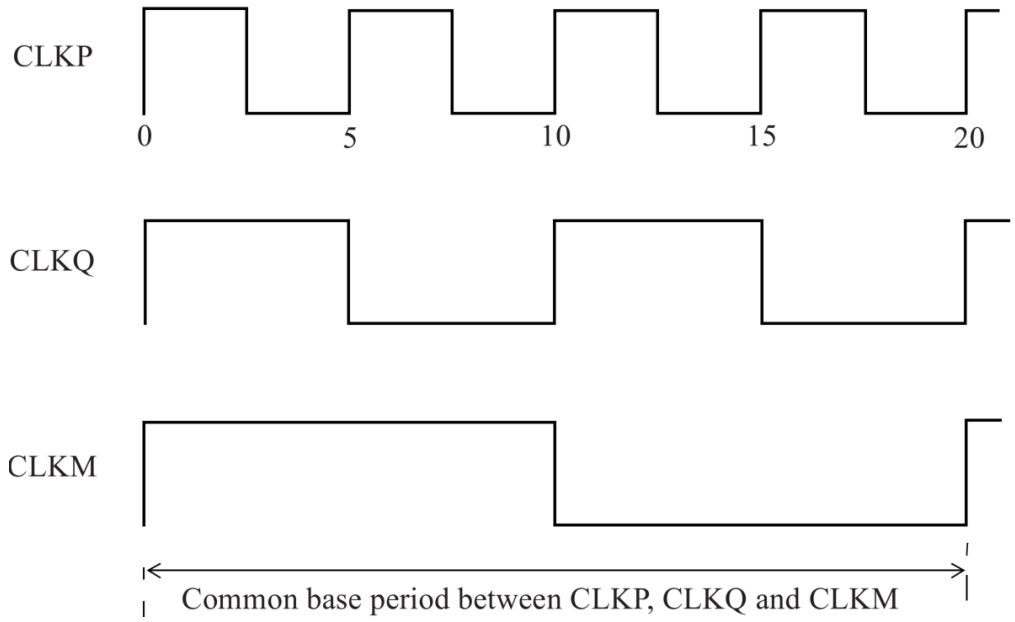
In such cases, STA is performed by computing **a common base period among all related clocks** (two clocks are related if they have a data path between their domains).

The common base period is established so that all clocks are synchronized.

1- Integer Multiples

Here is an example that shows four related clocks:

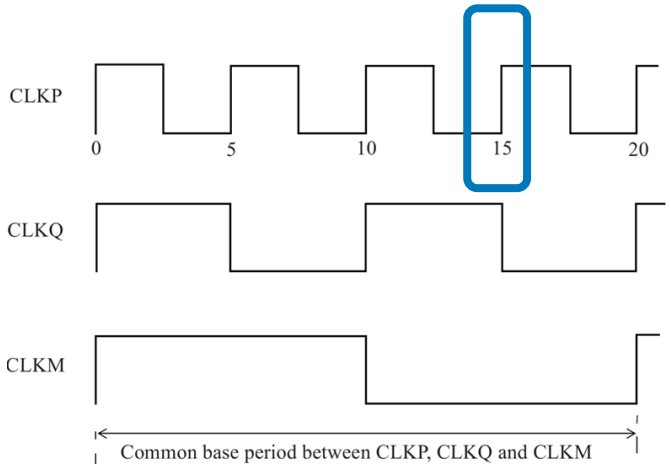
```
create_clock -name CLKM \
  -period 20 -waveform {0 10} [get_ports CLKM]
create_clock -name CLKQ -period 10 -waveform {0 5}
create_clock -name CLKP \
  -period 5 -waveform {0 2.5} [get_ports CLKP]
```



Multiple Clocks

1- Integer Multiples

Here is a setup timing report for a path that goes from the faster clock to the slower clock.



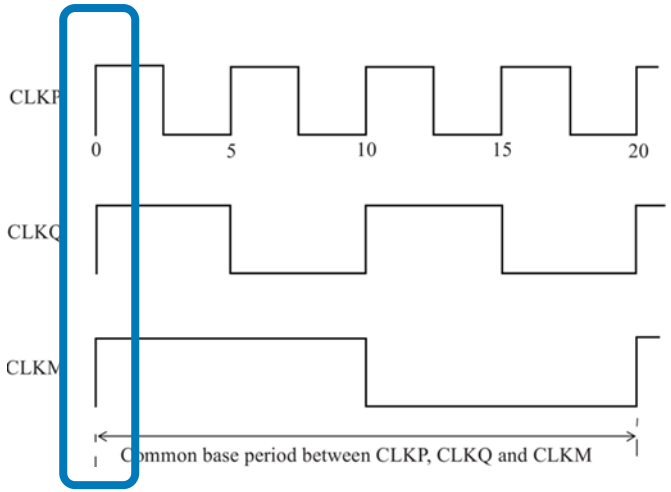

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (rise edge)                            15.00      15.00
  clock source latency                               0.00      15.00
  CLKP (in)                                          0.00      15.00 r
  UCKBUF4/C (CKB  )                                  0.07      15.07 r
  UFF3/CK (DFF )                                     0.00      15.07 r
  UFF3/Q (DFF ) <-                                   0.15      15.22 f
  UNOR0/ZN (NR2  )                                   0.05      15.27 r
  UBUF4/Z (BUFF  )                                   0.05      15.32 r
  UFF1/D (DFF )                                      0.00      15.32 r
  data arrival time                                            15.32
```

1- Integer Multiples

```
clock CLKM (rise edge)                    20.00       20.00
clock source latency                       0.00       20.00
CLKM (in)                                  0.00       20.00 r
UCKBUF0/C (CKB  )                          0.06       20.06 r
UCKBUF2/C (CKB  )                          0.07       20.12 r
UFF1/CK (DFF )                             0.00       20.12 r
clock uncertainty                         -0.30       19.82
library setup time                        -0.04       19.78
data required time                                    19.78
-----------------------------------------------------------
data required time                                    19.78
data arrival time                                    -15.32
-----------------------------------------------------------
slack (MET)                                            4.46
```

1- Integer Multiples

Here is the corresponding hold path report..



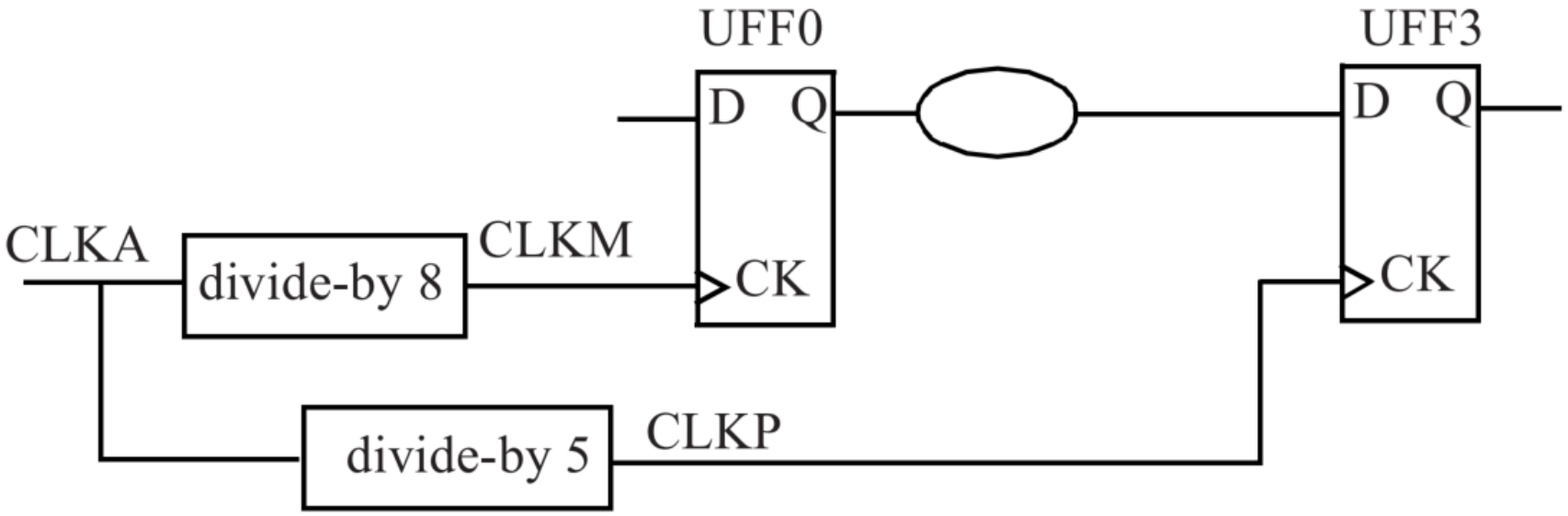

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
Path Group: CLKM
Path Type: min

Point                                              Incr       Path
-----------------------------------------------------------------------
clock CLKP (rise edge)                             0.00       0.00
clock source latency                               0.00       0.00
CLKP (in)                                          0.00       0.00 r
UCKBUF4/C (CKB  )                                  0.07       0.07 r
UFF3/CK (DFF )                                     0.00       0.07 r
UFF3/Q (DFF ) <-                                   0.16       0.22 r
UNOR0/ZN (NR2  )                                   0.02       0.25 f
UBUF4/Z (BUFF  )                                   0.06       0.30 f
UFF1/D (DFF )                                      0.00       0.30 f
data arrival time                                             0.30
```

1- Integer Multiples

```
clock CLKM (rise edge)                          0.00          0.00
clock source latency                            0.00          0.00
CLKM (in)                                       0.00          0.00 r
UCKBUF0/C (CKB  )                               0.06          0.06 r
UCKBUF2/C (CKB  )                               0.07          0.12 r
UFF1/CK (DFF )                                  0.00          0.12 r
clock uncertainty                               0.05          0.17
library hold time                               0.01          0.19
data required time                                            0.19
-------------------------------------------------------------------
data required time                                            0.19
data arrival time                                            -0.30
-------------------------------------------------------------------
slack (MET)                                                   0.12
```

2 Non-Integer Multiples

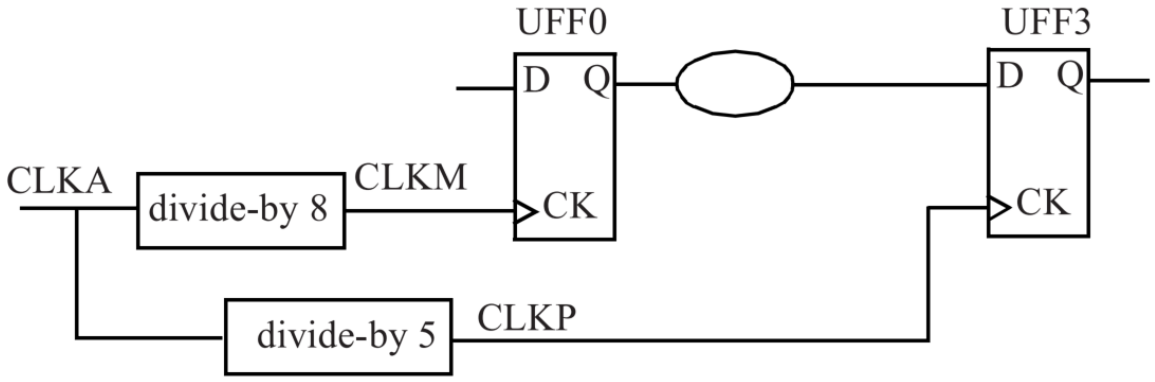
Consider the case when there is a data path between two clock domains whose frequencies are not multiples of each other.



2 Non-Integer Multiples

Here are the clock definitions (waveforms are shown in Figure 8-35)

```
create_clock -name CLKM \
  -period 8 -waveform {0 4} [get_ports CLKM]
create_clock -name CLKQ -period 10 -waveform {0 5}
create_clock -name CLKP \
  -period 5 -waveform {0 2.5} [get_ports CLKP]
```

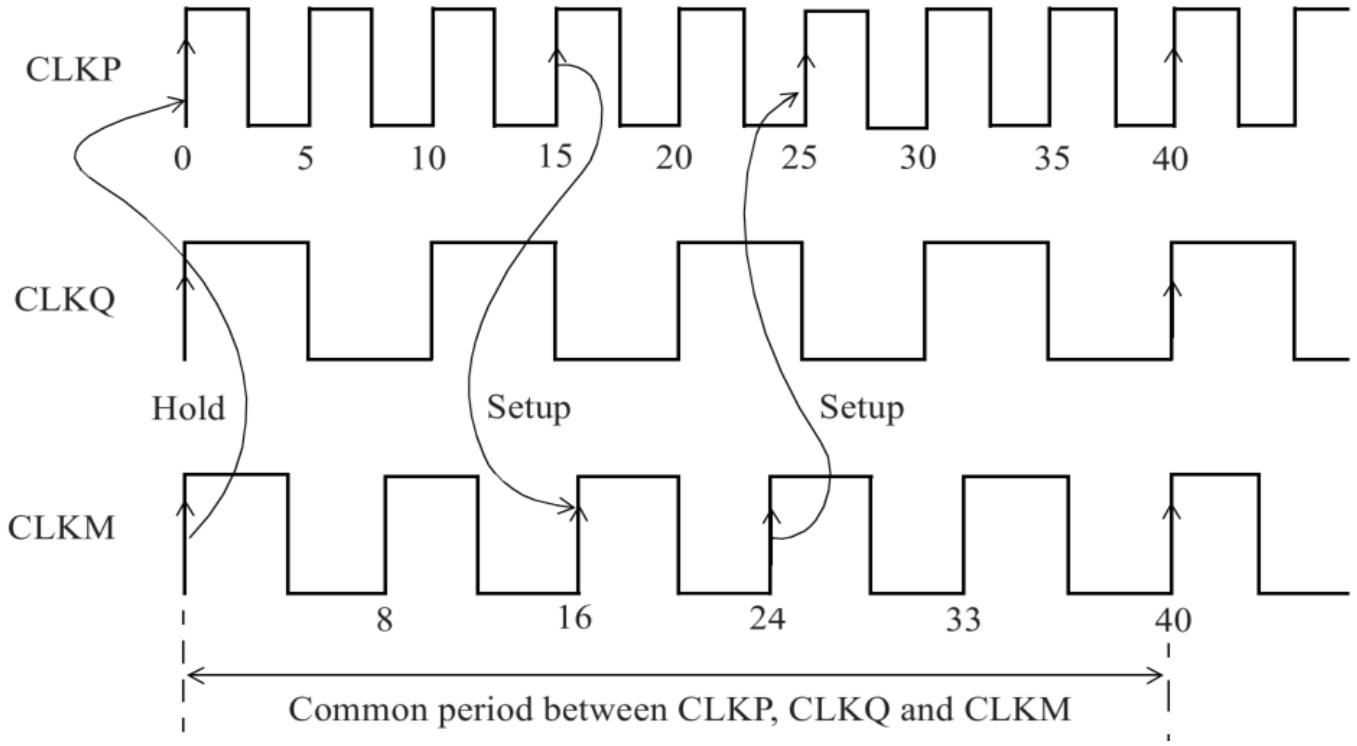


2 Non-Integer Multiples

The timing analysis process computes **a common period for the related clocks**, and the clocks are then expanded to this base period.

Note that the common period is found only for related clocks (that is, clocks that have timing paths between them).

2 Non-Integer Multiples



The setup check occurs over the minimum time between the launch edge and the capture edge of the clock.

2 Non-Integer Multiples

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: max

  Point                                          Incr       Path
  -----------------------------------------------------------------
  clock CLKM (rise edge)                        24.00      24.00
  clock source latency                           0.00      24.00
  CLKM (in)                                      0.00      24.00 r
  UCKBUF0/C (CKB  )                              0.06      24.06 r
  UCKBUF1/C (CKB  )                              0.06      24.11 r
  UFF0/CK (DFF )                                 0.00      24.11 r
  UFF0/Q (DFF ) <-                               0.14      24.26 f
  UNAND0/ZN (ND2  )                              0.03      24.29 r
  UFF3/D (DFF )                                  0.00      24.29 r
  data arrival time                                        24.29
```

2 Non-Integer Multiples

```
clock CLKP (rise edge)                    25.00       25.00
clock source latency                       0.00       25.00
CLKP (in)                                  0.00       25.00 r
UCKBUF4/C (CKB  )                          0.07       25.07 r
UFF3/CK (DFF )                             0.00       25.07 r
clock uncertainty                         -0.30       24.77
library setup time                        -0.04       24.72
data required time                                    24.72
-------------------------------------------------------------
data required time                                    24.72
data arrival time                                    -24.29
-------------------------------------------------------------
slack (MET)                                           0.44
```

2 Non-Integer Multiples

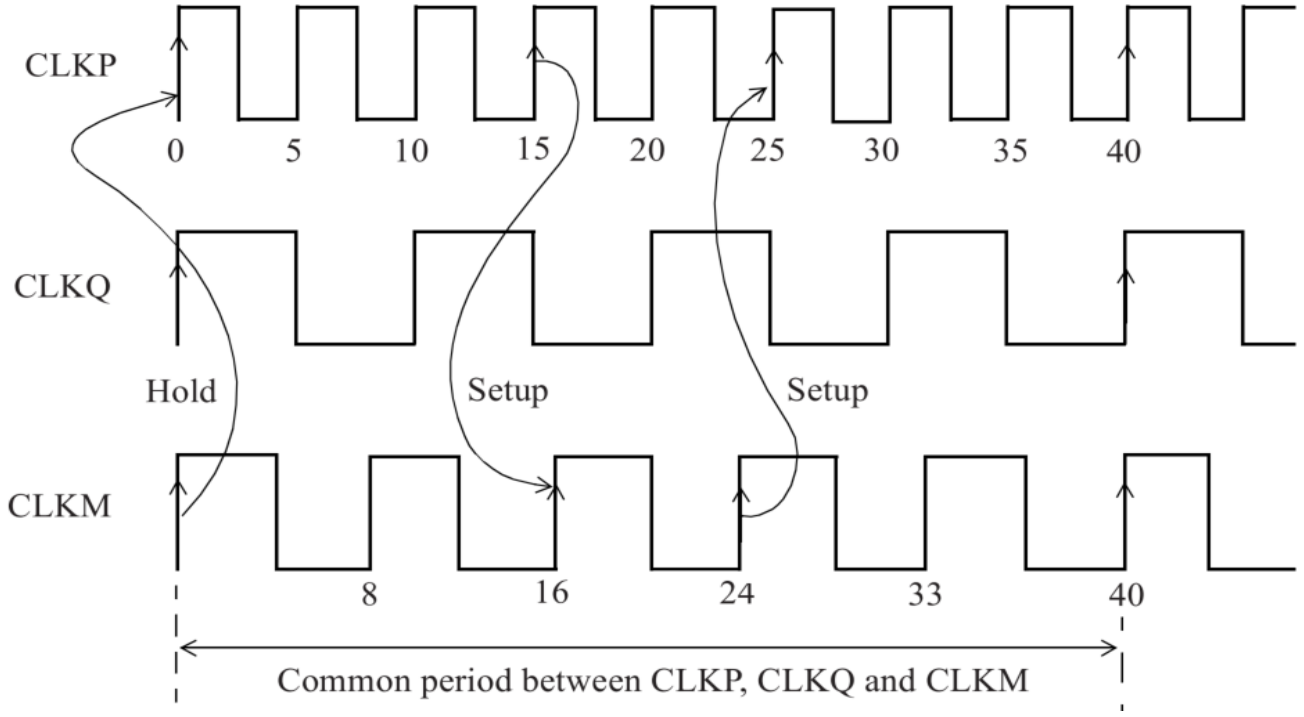
```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Path Group: CLKP
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKM (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKM (in)                                          0.00       0.00 r
  UCKBUF0/C (CKB  )                                  0.06       0.06 r
  UCKBUF1/C (CKB  )                                  0.06       0.11 r
  UFF0/CK (DFF )                                     0.00       0.11 r
  UFF0/Q (DFF ) <-                                   0.14       0.26 r
  UNAND0/ZN (ND2  )                                  0.03       0.29 f
  UFF3/D (DFF )                                      0.00       0.29 f
  data arrival time                                             0.29
```

2 Non-Integer Multiples

clock CLKP (rise edge)	**0.00**	0.00	
clock source latency	0.00	0.00	
CLKP (in)	0.00	0.00	r
UCKBUF4/C (CKB)	0.07	0.07	r
UFF3/CK (DFF)	0.00	0.07	r
clock uncertainty	0.05	0.12	
library **hold** time	0.02	0.13	
data required time		0.13	
data required time		0.13	
data arrival time		-0.29	
slack (MET)		0.16	

2 Non-Integer Multiples

Now we examine the setup path from the CLKP clock domain to the CLKM clock domain. In this case, the most restrictive setup path is from a launch edge at 15ns of clock CLKP to the capture edge at 16ns of clock CLKM.



2 Non-Integer Multiples

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: max

  Point                                          Incr       Path
  -----------------------------------------------------------------
  clock CLKP (rise edge)                        15.00      15.00
  clock source latency                           0.00      15.00
  CLKP (in)                                      0.00      15.00 r
  UCKBUF4/C (CKB  )                              0.07      15.07 r
  UFF3/CK (DFF )                                 0.00      15.07 r
  UFF3/Q (DFF ) <-                               0.15      15.22 f
  UNOR0/ZN (NR2  )                               0.05      15.27 r
  UBUF4/Z (BUFF  )                               0.05      15.32 r
  UFF1/D (DFF )                                  0.00      15.32 r
  data arrival time                                        15.32
```

2 Non-Integer Multiples

```
clock CLKM (rise edge)                          16.00       16.00
clock source latency                             0.00       16.00
CLKM (in)                                        0.00       16.00 r
UCKBUF0/C (CKB  )                                0.06       16.06 r
UCKBUF2/C (CKB  )                                0.07       16.12 r
UFF1/CK (DFF )                                   0.00       16.12 r
clock uncertainty                               -0.30       15.82
library setup time                              -0.04       15.78
data required time                                          15.78
-----------------------------------------------------------------
data required time                                          15.78
data arrival time                                          -15.32
-----------------------------------------------------------------
slack (MET)                                                  0.46
```

2 Non-Integer Multiples

```
Startpoint: UFF3 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKP (in)                                          0.00       0.00 r
  UCKBUF4/C (CKB  )                                  0.07       0.07 r
  UFF3/CK (DFF )                                     0.00       0.07 r
  UFF3/Q (DFF ) <-                                   0.16       0.22 r
  UNOR0/ZN (NR2  )                                   0.02       0.25 f
  UBUF4/Z (BUFF  )                                   0.06       0.30 f
  UFF1/D (DFF )                                      0.00       0.30 f
  data arrival time                                             0.30
```

2 Non-Integer Multiples

```
clock CLKM (rise edge)                          0.00          0.00
clock source latency                            0.00          0.00
CLKM (in)                                       0.00          0.00 r
UCKBUF0/C (CKB  )                               0.06          0.06 r
UCKBUF2/C (CKB  )                               0.07          0.12 r
UFF1/CK (DFF )                                  0.00          0.12 r
clock uncertainty                               0.05          0.17
library hold time                               0.01          0.19
data required time                                            0.19
-------------------------------------------------------------------
data required time                                            0.19
data arrival time                                            -0.30
-------------------------------------------------------------------
slack (MET)                                                   0.12
```

3 Phase Shifted

Here is an example where two clocks are ninety degrees phase-shifted with respect to each other.

```
create_clock -period 2.0 -waveform {0 1.0} [get_ports CKM]
create_clock -period 2.0 -waveform {0.5 1.5} \
  [get_ports CKM90]
```

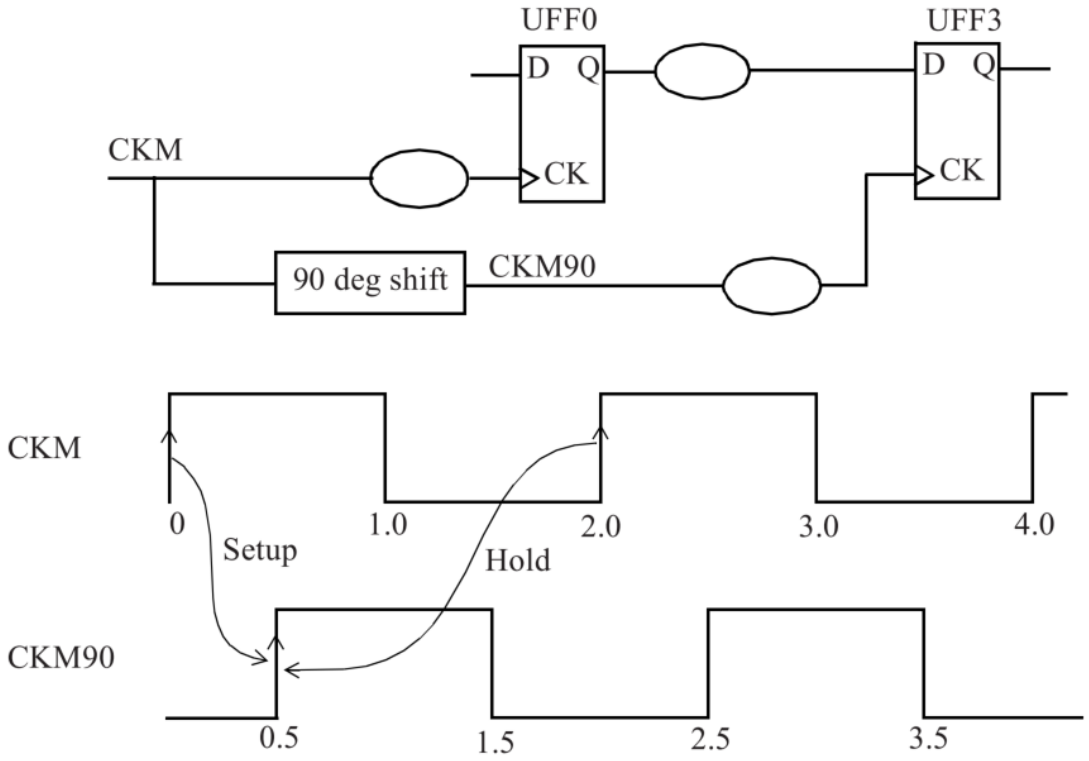


Figure 8-36 *Phase-shifted clocks.*

3 Phase Shifted

Startpoint: UFF0 (rising edge-triggered flip-flop clocked by **CKM**)
Endpoint: UFF3 (rising edge-triggered flip-flop clocked by **CKM90**)
  Path Group: **CKM90**
  Path Type: **max**

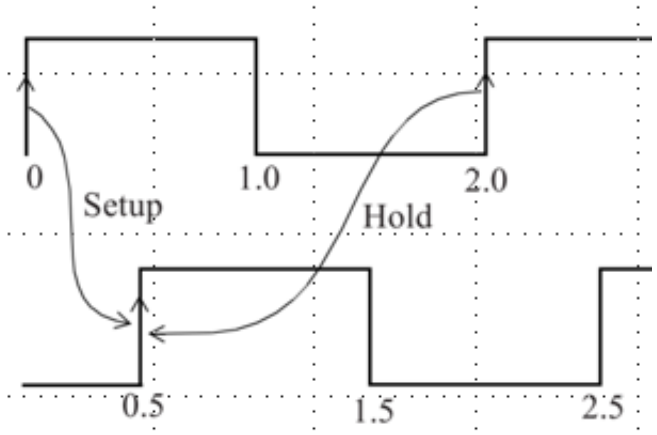
Point	Incr	Path
clock CKM (rise edge)	**0.00**	0.00
clock source latency	0.00	0.00
CKM (in)	0.00	0.00 r
UCKBUF0/C (CKB)	0.06	0.06 r
UCKBUF1/C (CKB)	0.06	0.11 r
UFF0/CK (DF)	0.00	0.11 r
UFF0/Q (DF) <-	0.14	0.26 f
UNAND0/ZN (ND2)	0.03	0.29 r
UFF3/D (DF)	0.00	0.29 r
data arrival time		0.29

3 Phase Shifted

```
clock CKM90(rise edge)                    0.50        0.50
clock source latency                      0.00        0.50

CKM90(in)                                 0.00        0.50 r
UCKBUF4/C (CKB  )                         0.07        0.57 r
UFF3/CK (DF  )                            0.00        0.57 r
clock uncertainty                        -0.30        0.27
library setup time                       -0.04        0.22
data required time                                    0.22
-------------------------------------------------------------
data required time                                    0.22
data arrival time                                    -0.29
-------------------------------------------------------------
slack (VIOLATED)                                     -0.06
```

Multiple Clocks

3 Phase Shifted



Startpoint: UFF0 (rising edge-triggered flip-flop clocked by **CKM**)
Endpoint: UFF3 (rising edge-triggered flip-flop clocked by **CKM90**)
  Path Group: **CKM90**
  Path Type: **min**

Point	Incr	Path
clock CKM (rise edge)	**2.00**	2.00
clock source latency	0.00	2.00
CKM (in)	0.00	2.00 r
UCKBUF0/C (CKB)	0.06	2.06 r
UCKBUF1/C (CKB)	0.06	2.11 r
UFF0/CK (DF)	0.00	2.11 r
UFF0/Q (DF) <-	0.14	2.26 r
UNAND0/ZN (ND2)	0.03	2.29 f
UFF3/D (DF)	0.00	2.29 f
data arrival time		2.29

3 Phase Shifted

clock CKM90(rise edge)	**0.50**	0.50	
clock source latency	0.00	0.50	
CLM90(in)	0.00	0.50	r
UCKBUF4/C (CKB)	0.07	0.57	r
UFF3/CK (DF)	0.00	0.57	r
clock uncertainty	0.05	0.62	
library **hold** time	0.02	0.63	
data required time		0.63	
data required time		0.63	
data arrival time		-2.29	
slack (MET)		1.66	

参考书目

- Static Timing Analysis for Nanometer Designs: A Practical Approach. J. Bhasker, Rakesh Chadha. Springer Science Business Media, LLC 2009.
- 集成电路静态时序分析与建模. 刘峰, 机械工业出版社.出版时间：2016-07-01.

谢谢聆听！

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