数字集成电路静态时序分析基础

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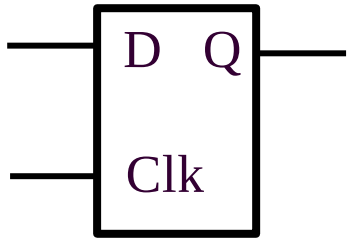
CONTENT

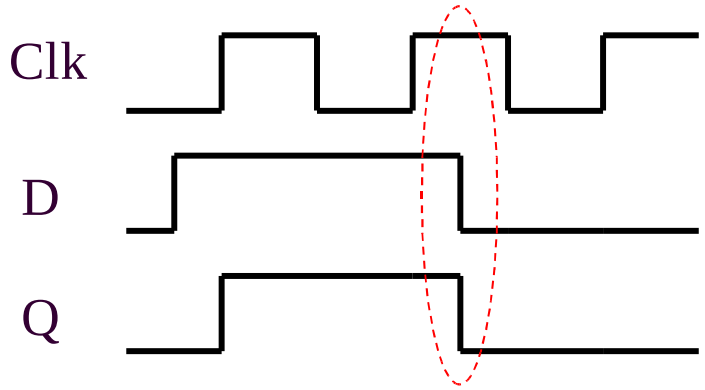
Part 6: Robust Verification

- **Time Borrowing**

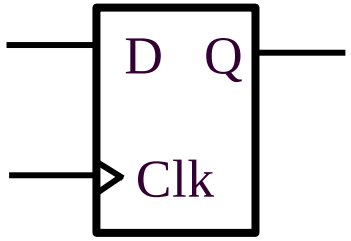
Time Borrowing

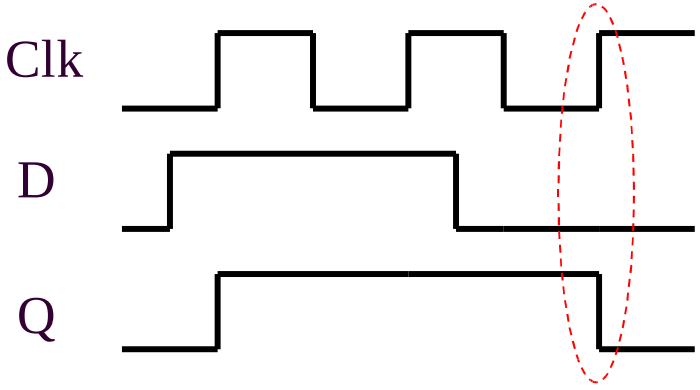
Latch





DFF

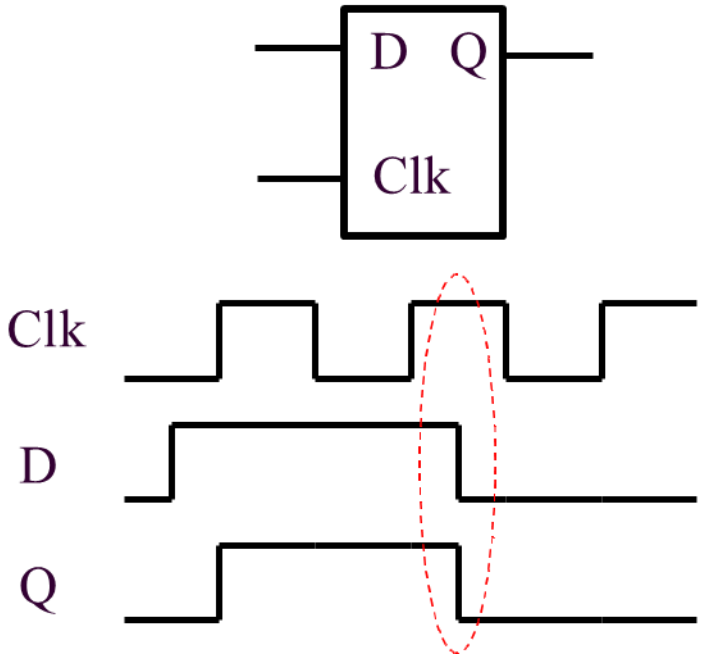




Time Borrowing

The time borrowing technique, which is also called cycle stealing, occurs at a latch.

- In a latch, one edge of the clock makes the latch transparent, that is, it opens the latch so that output of the latch is the same as the data input; this clock edge is called the opening edge.
- The second edge of the clock closes the latch, that is, any change on the data input is no longer available at the output of the latch; this clock edge is called the closing edge.



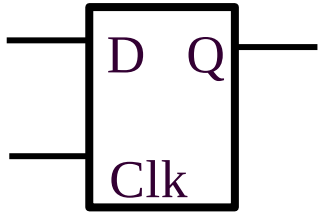
Time Borrowing

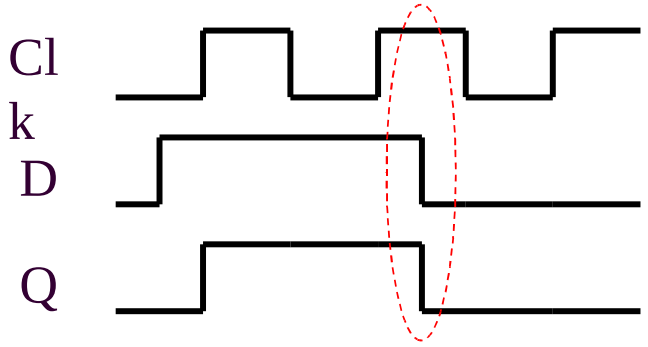
Typically, the data should be ready at a latch input before the active edge of the clock.

However, since a latch is transparent when the clock is active, the data can arrive later than the active clock edge, that is, it can borrow time from the next cycle.

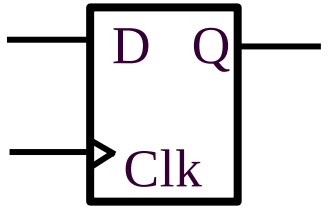
If such time is borrowed, the time available for the following stage (latch to another sequential cell) is reduced.

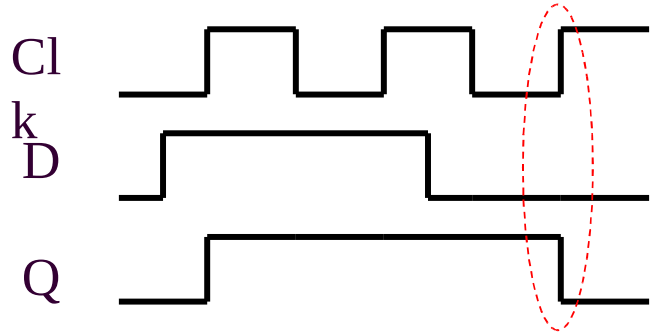
Latch





DFF



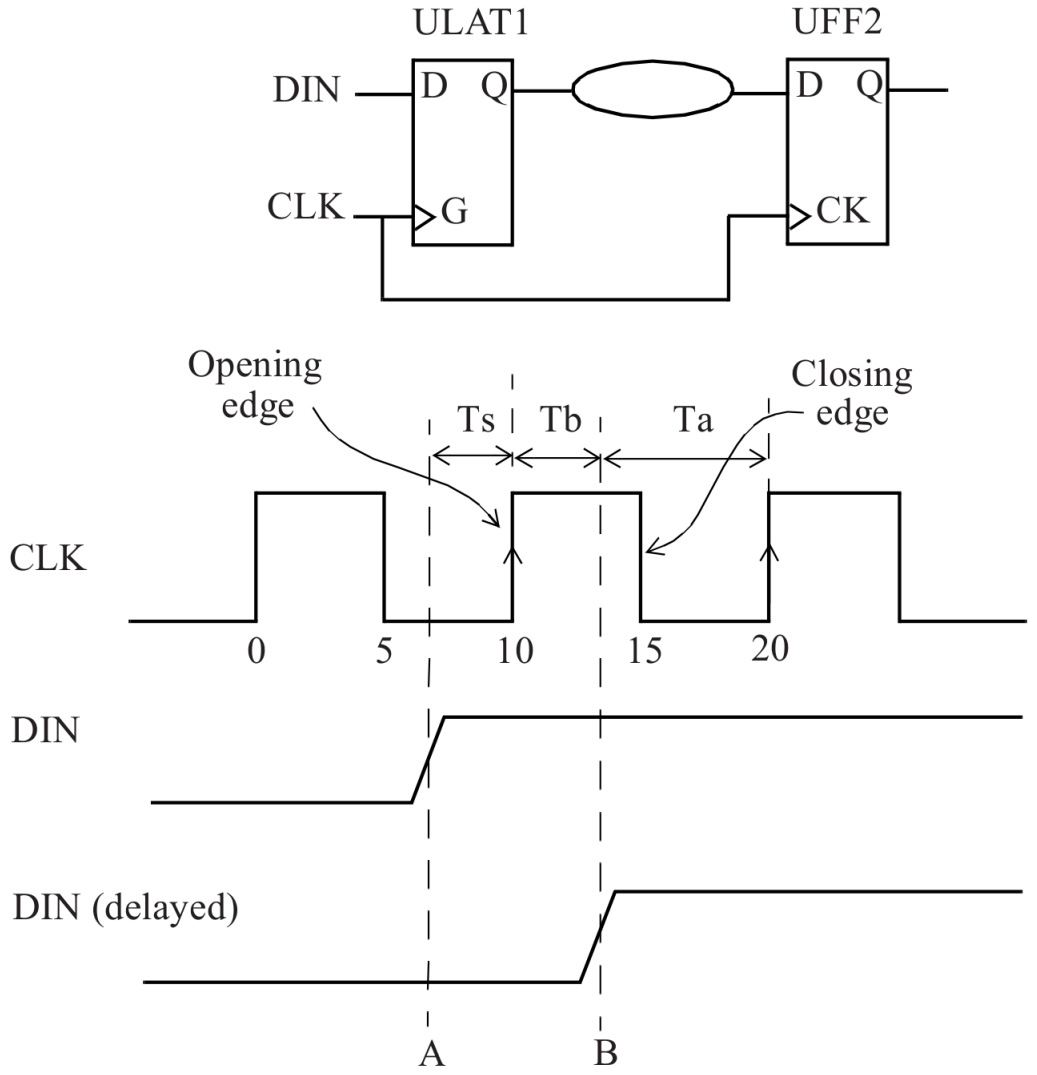


Time Borrowing

Here is an example of time borrowing using an active rising edge.

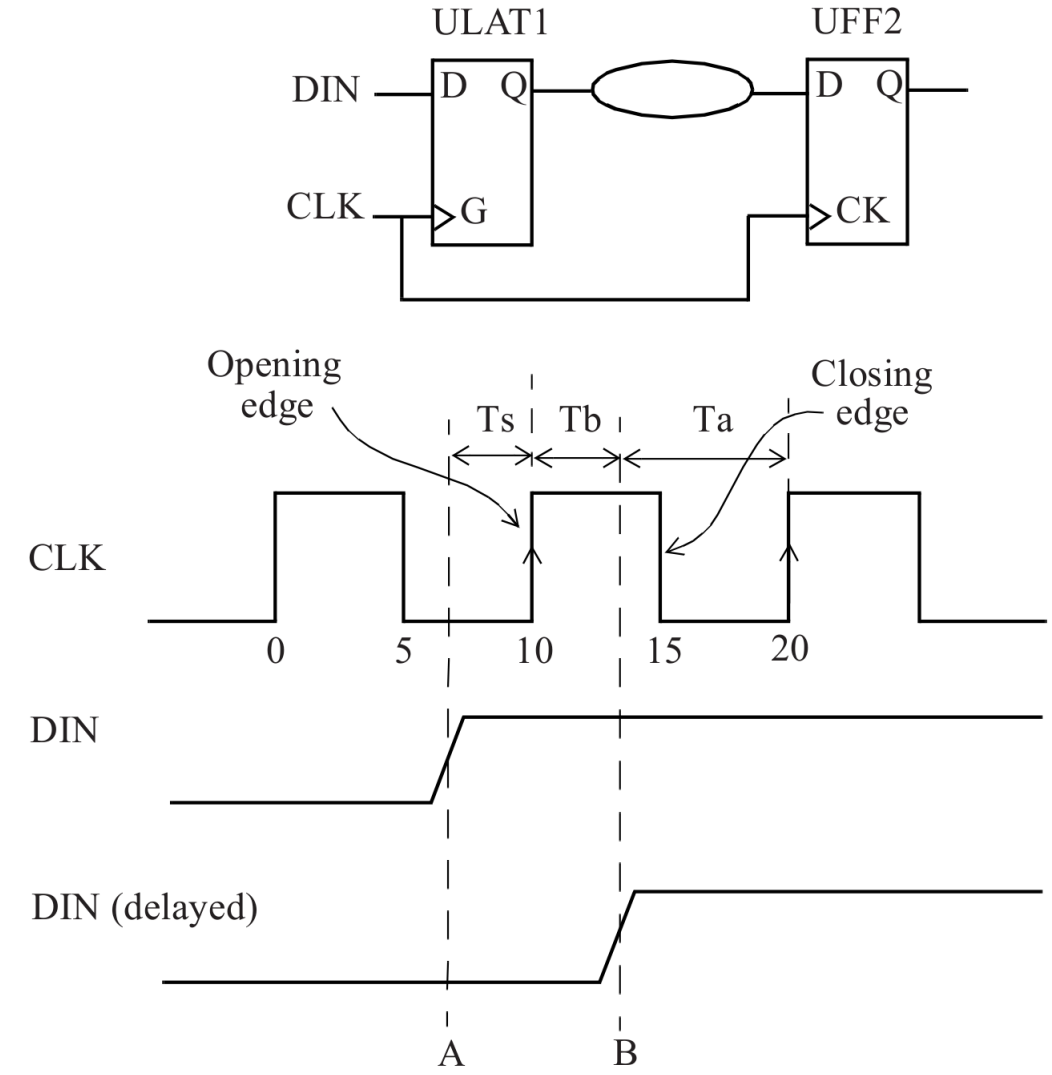
- If data DIN is ready at time A prior to the latch opening on the rising edge of CLK at 10ns, the data flows to the output of the latch as it opens.

If data arrives at time B as shown for DIN (delayed), it borrows time Tb. However, this reduces the time available from the latch to the next flip-flop UFF2 - instead of a complete clock cycle, only time Ta is available.



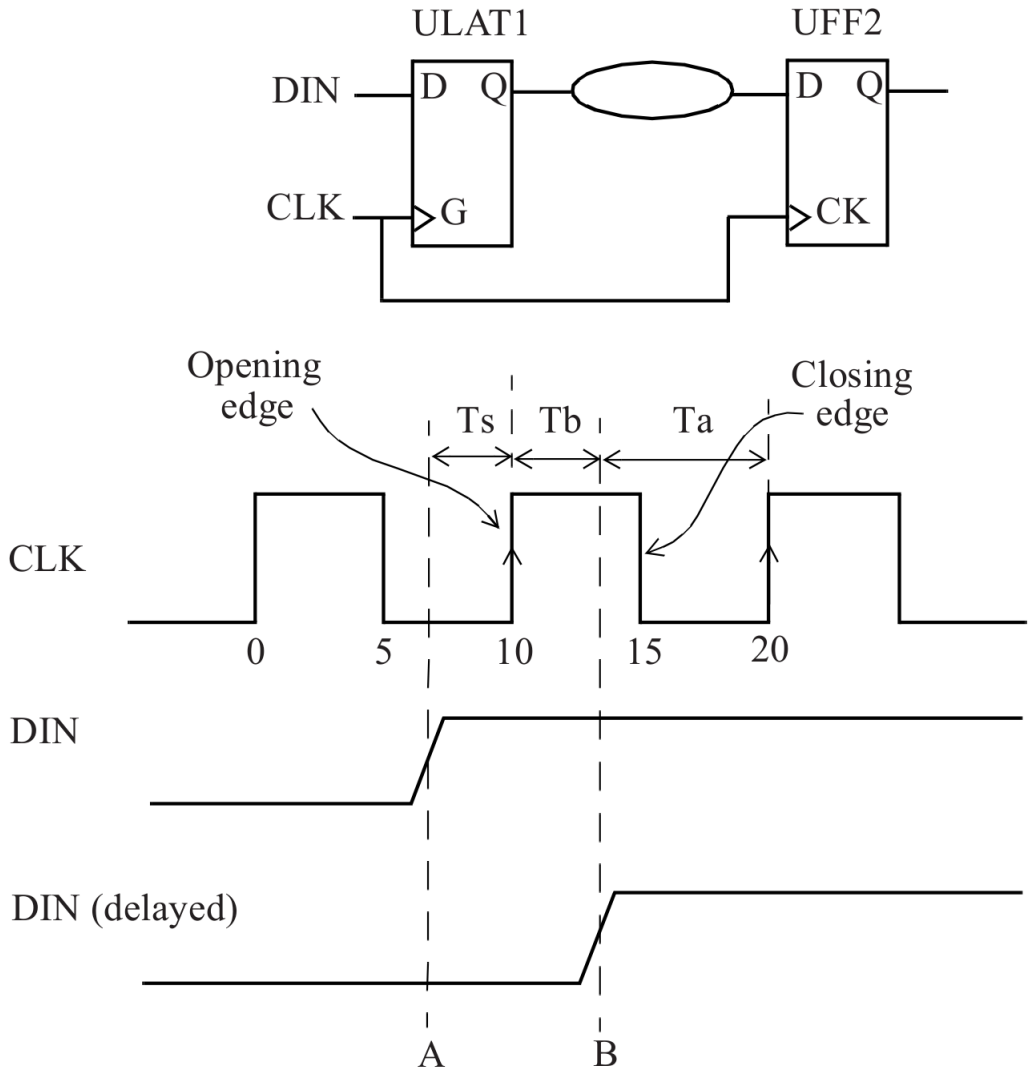
Time Borrowing

- The first rule in timing to a latch is that if the data arrives before the opening edge of the latch, the behavior is modeled exactly like a flip-flop.
- The opening edge captures the data and the same clock edge launches the data as the start point for the next path.



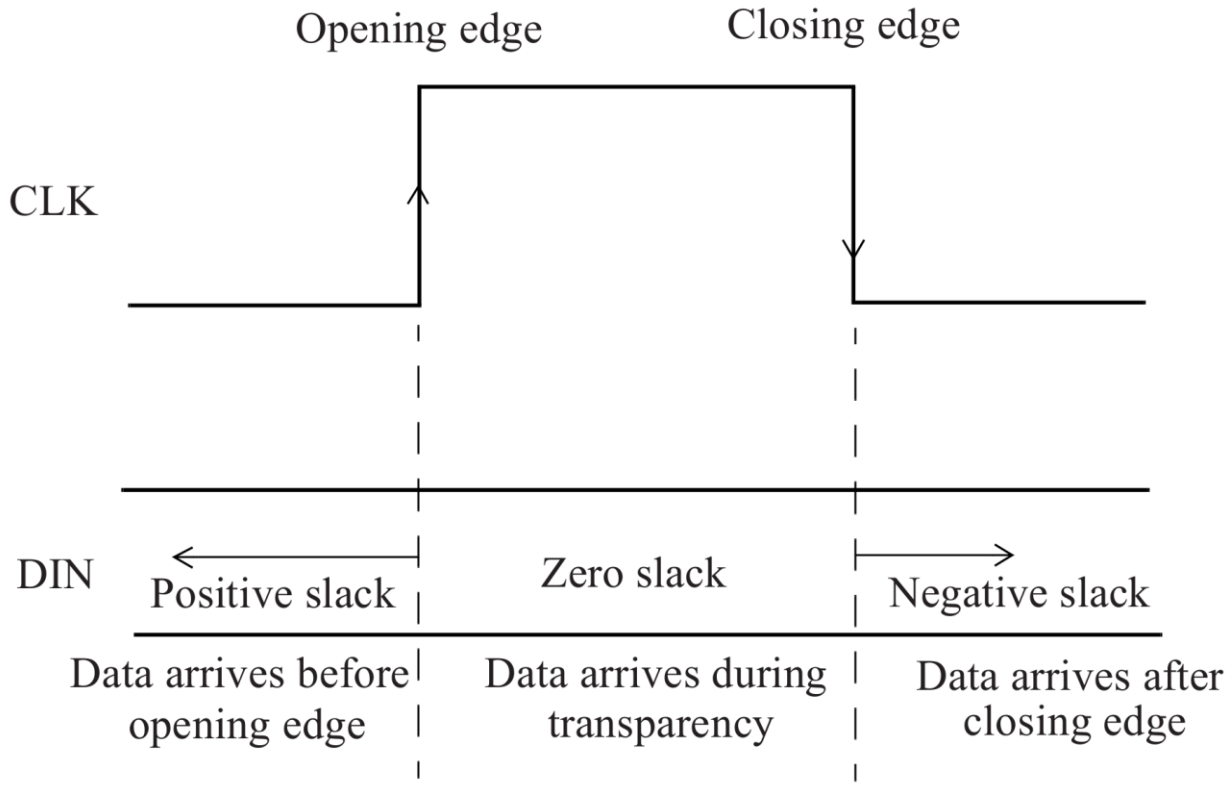
Time Borrowing

- The second rule applies when the data signal arrives while the latch is transparent (between the opening and the closing edge).
- The output of the latch, rather than the clock pin, is used as the launch point for the next stage.
- The amount of time borrowed by the path ending at the latch determines the launch time for the next stage.



Time Borrowing

The timing regions for data arrival for positive slack, zero slack, and negative slack (that is, when a violation occurs).

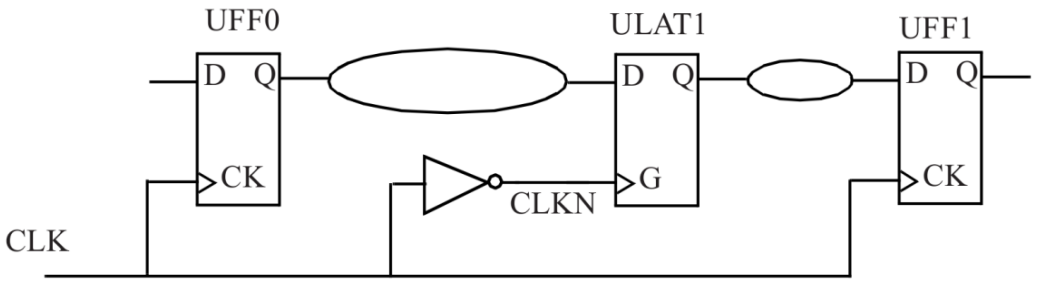


A data signal that arrives after the closing edge at the latch is a timing violation.

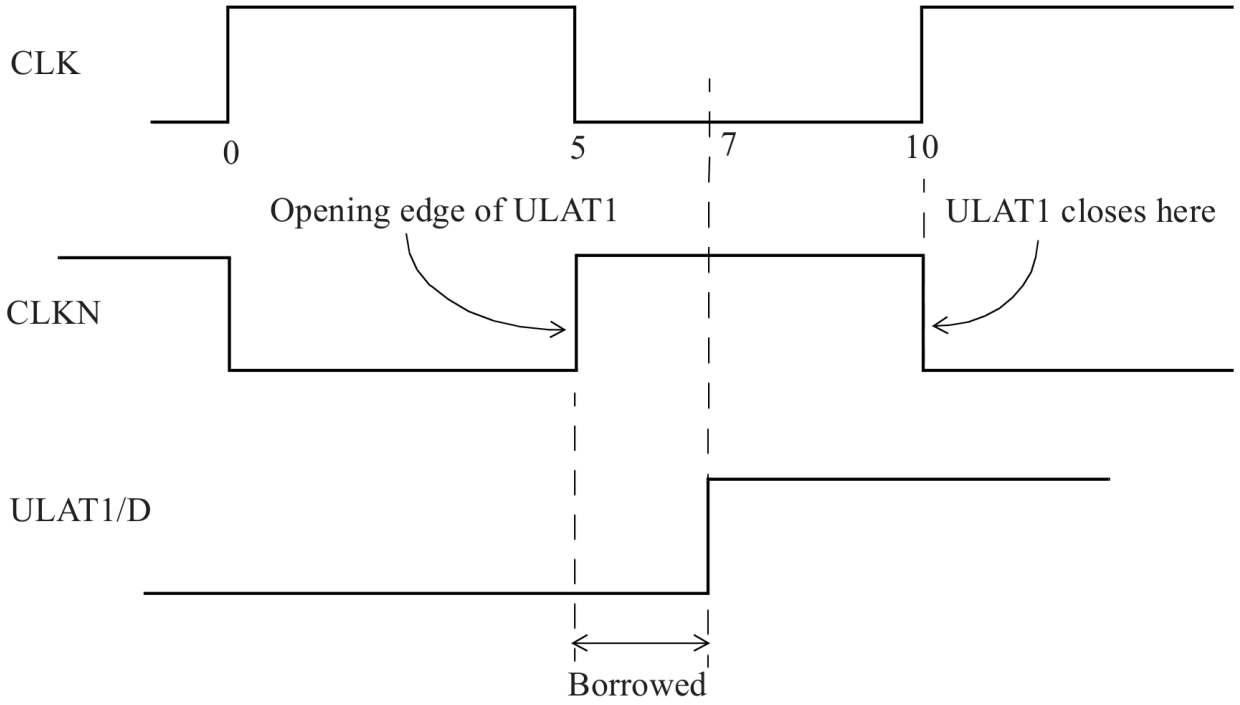
Time Borrowing

This is the use of a latch with a half-cycle path to the next stage flip-flop.

We next describe three sets of timing reports for the latch example of it to illustrate the different amounts of time borrowed from the next stage.



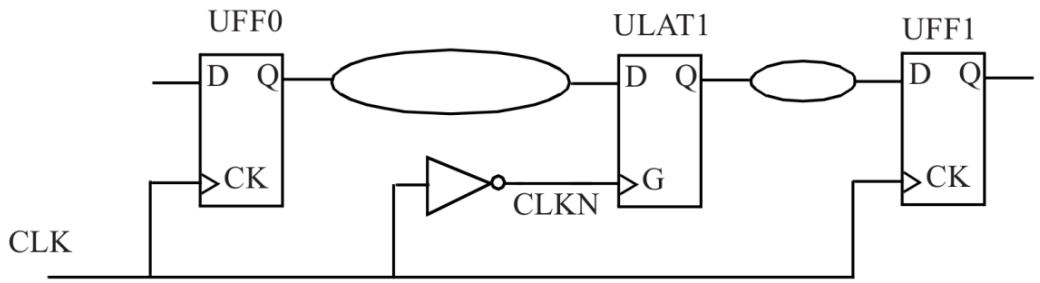
(a) Logic.



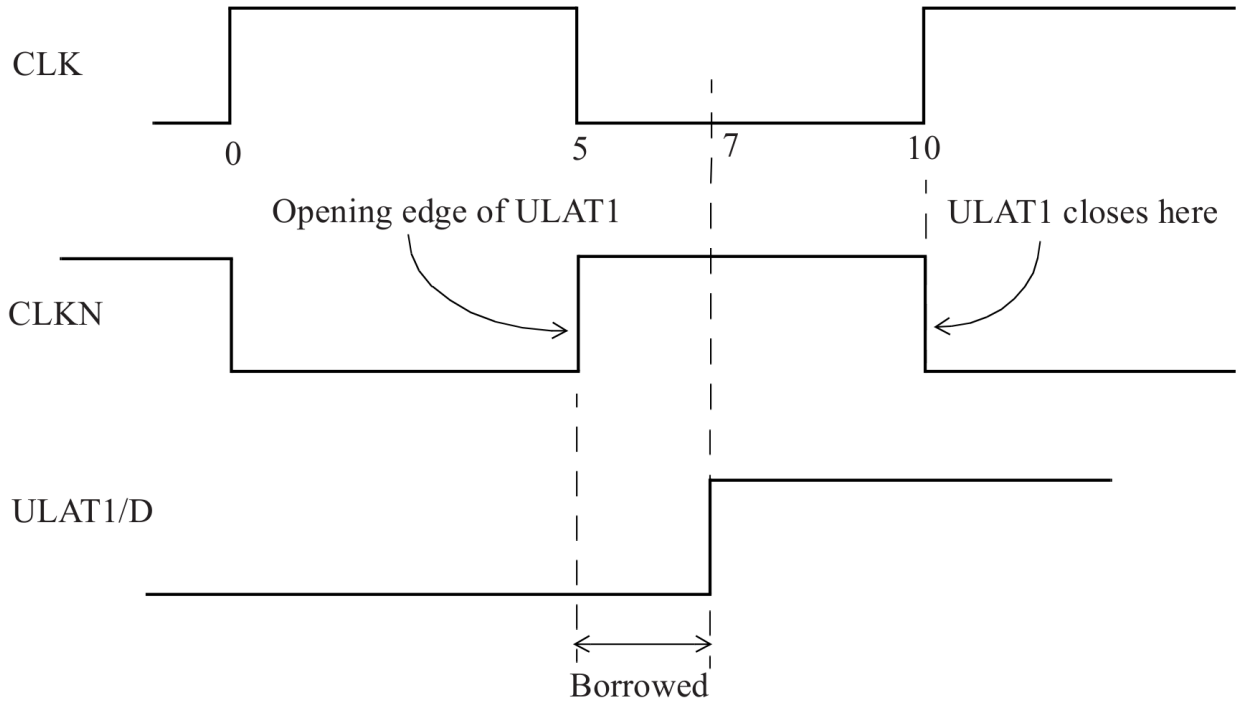
(b) Clock and data waveforms for 7ns data path.

Time Borrowing

Here is the setup path report when the data path delay from the flip-flop *UFF0* to the latch *ULAT1* is less than 5ns.

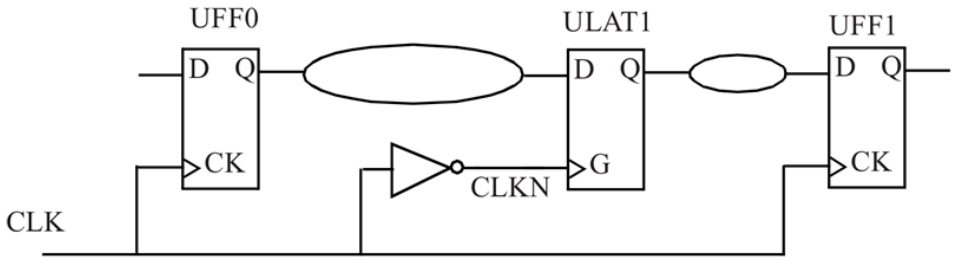


(a) Logic.

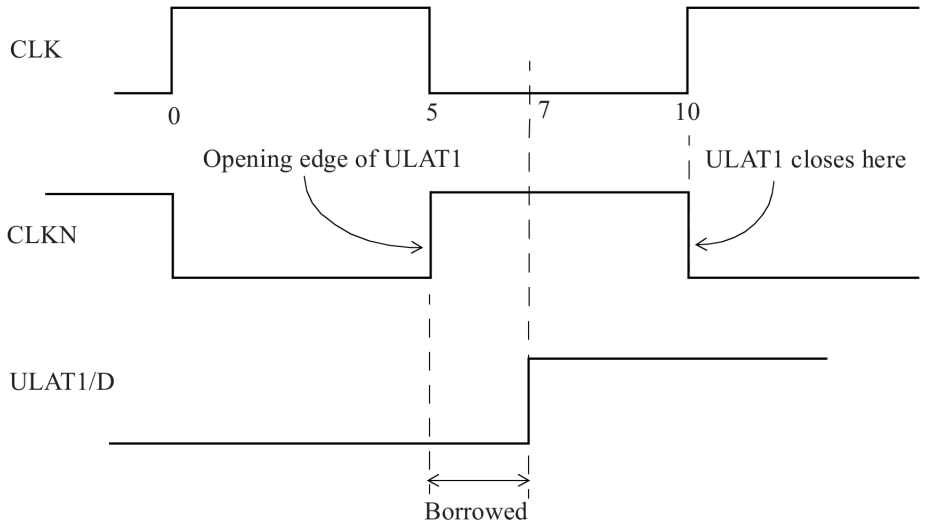


(b) Clock and data waveforms for 7ns data path.

Time Borrowing



(a) Logic.



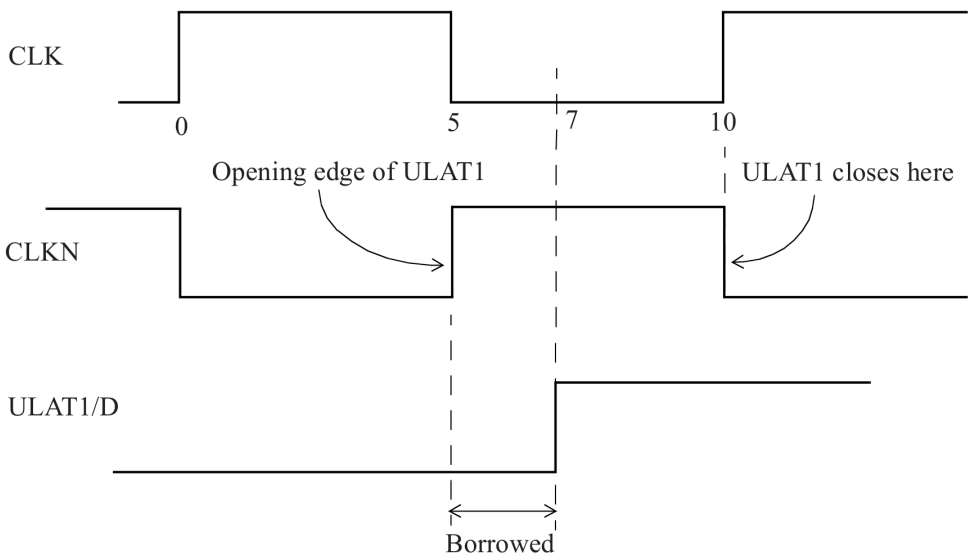
(b) Clock and data waveforms for 7ns data path.

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: ULAT1 (positive level-sensitive latch clocked by CLK')
  Path Group: CLK
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------
  clock CLK (rise edge)                              0.00       0.00
  clock source latency                               0.00       0.00

  clk (in)                                           0.00       0.00 r
  UFF0/CK (DF  )                                     0.00       0.00 r
  UFF0/Q (DF  )                                      0.12       0.12 r
  UBUF0/Z (BUFF  )                                   2.01       2.13 r
  UBUF1/Z (BUFF  )                                   2.46       4.59 r
  UBUF2/Z (BUFF  )                                   0.07       4.65 r
  ULAT1/D (LH  )                                     0.00       4.65 r
  data arrival time                                             4.65
```

Time Borrowing



(b) Clock and data waveforms for 7ns data path.

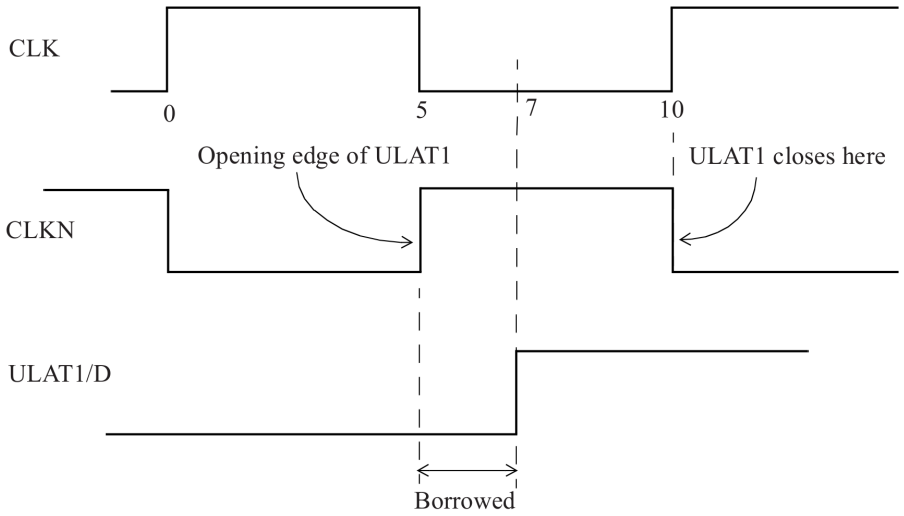
In this case, there is no need to borrow as data reaches the latch ULAT1 in time before the latch opens.

```
clock CLK' (rise edge)                    5.00        5.00
clock source latency                      0.00        5.00
clk (in)                                  0.00        5.00 f
UINV0/ZN (INV  )                          0.02        5.02 r
ULAT1/G (LH  )                            0.00        5.02 r
time borrowed from endpoint               0.00        5.02
data required time                                    5.02
-------------------------------------------------------------
data required time                                    5.02
data arrival time                                    -4.65
-------------------------------------------------------------
slack (MET)                                           0.36

Time Borrowing Information
-------------------------------------------------------
CLK' nominal pulse width                  5.00
clock latency difference                 -0.00
library setup time                       -0.01
-------------------------------------------------------
max time borrow                           4.99
actual time borrow                        0.00
-------------------------------------------------------
```

Time Borrowing

The path report below shows the case where the data path delay from the flip-flop UFF0 to the latch ULAT1 is **greater than 5ns**.

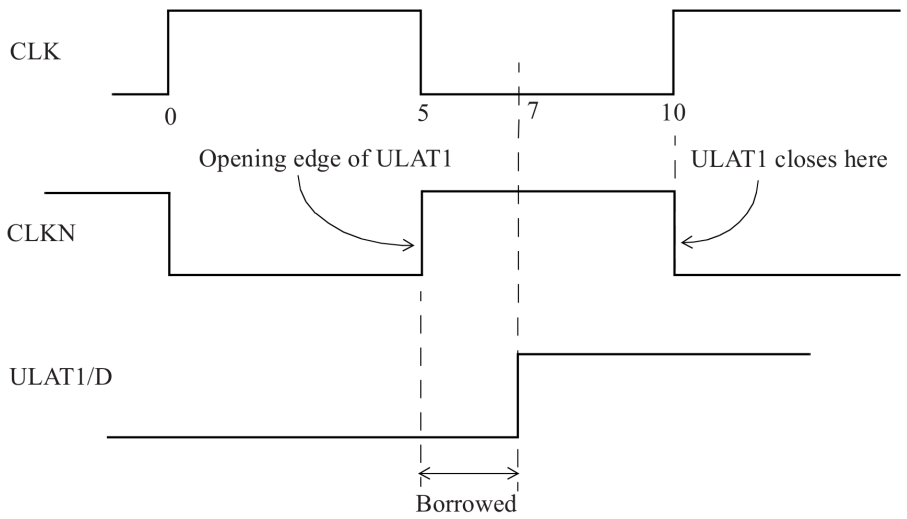


(b) Clock and data waveforms for 7ns data path.

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: ULAT1 (positive level-sensitive latch clocked by CLK')
  Path Group: CLK
  Path Type: max

  Point                                              Incr       Path
  ---------------------------------------------------------------------
  clock CLK (rise edge)                              0.00       0.00
  clock source latency                               0.00       0.00
  clk (in)                                           0.00       0.00 r
  UFF0/CK (DF  )                                     0.00       0.00 r
  UFF0/Q (DF  )                                      0.12       0.12 r
  UBUF0/Z (BUFF  )                                   3.50       3.62 r
  UBUF1/Z (BUFF  )                                   3.14       6.76 r
  UBUF2/Z (BUFF  )                                   0.07       6.83 r
  ULAT1/D (LH  )                                     0.00       6.83 r
  data arrival time                                             6.83
```

Time Borrowing



(b) Clock and data waveforms for 7ns data path.

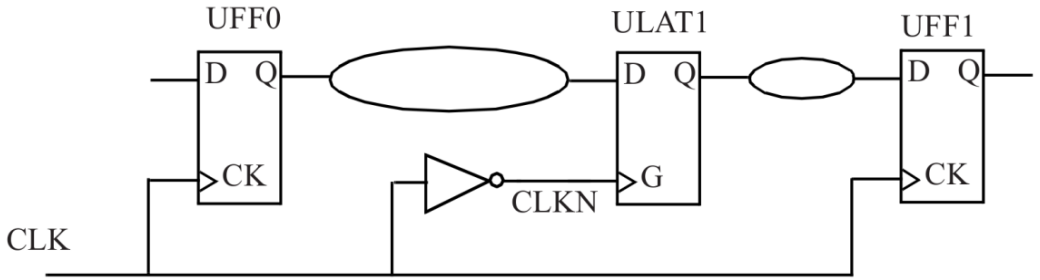
```
clock CLK' (rise edge)                          5.00       5.00
clock source latency                            0.00       5.00
clk (in)                                        0.00       5.00 f
UINV0/ZN (INV  )                                0.02       5.02 r
ULAT1/G (LH  )                                  0.00       5.02 r
time borrowed from endpoint                     1.81       6.83
data required time                                         6.83
-----------------------------------------------------------------
data required time                                         6.83
data arrival time                                         -6.83
-----------------------------------------------------------------
slack (MET)                                                0.00

Time Borrowing Information
-------------------------------------------------
CLK' nominal pulse width                        5.00
clock latency difference                       -0.00
library setup time                             -0.01
-------------------------------------------------
```

In this case, since the data becomes available while the latch is transparent, the required delay of 1.81ns is borrowed from the subsequent path and the timing is still met.

Time Borrowing

Here is the path report of the subsequent path showing that 1.81ns was already borrowed by the previous path.



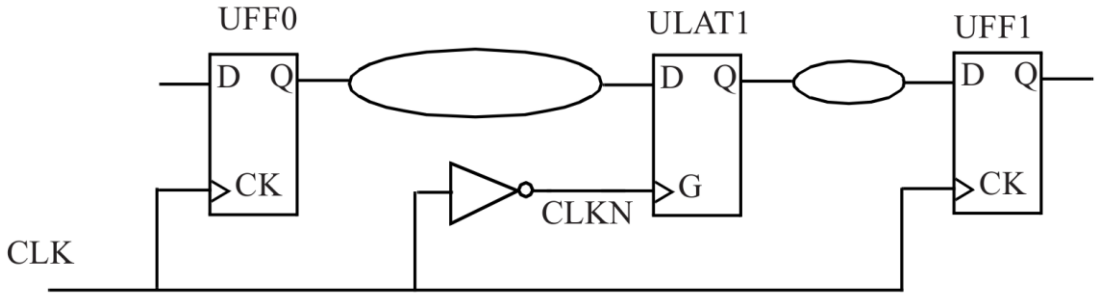
(a) Logic.

```
Startpoint: ULAT1 (positive level-sensitive latch clocked by CLK')
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLK' (rise edge)                             5.00       5.00
  clock source latency                               0.00       5.00
  clk (in)                                           0.00       5.00 f
  UINV0/ZN (INV  )                                   0.02       5.02 r
  ULAT1/G (LH  )                                     0.00       5.02 r
  time given to startpoint                           1.81       6.83
  ULAT1/QN (LH  )                                    0.13       6.95 f
  UFF1/D (DF  )                                      0.00       6.95 f
  data arrival time                                             6.95
```

Time Borrowing

Here is the path report of the subsequent path showing that 1.81ns was already borrowed by the previous path.



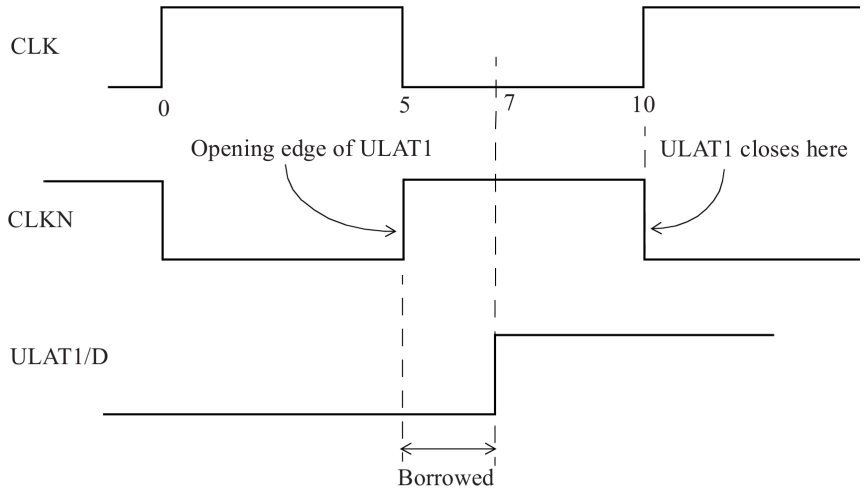
(a) Logic.

```
clock CLK (rise edge)                    10.00       10.00
clock source latency                      0.00       10.00
clk (in)                                  0.00       10.00 r
UFF1/CK (DF  )                            0.00       10.00 r
library setup time                       -0.04        9.96
data required time                                    9.96
-----------------------------------------------------------
data required time                                    9.96
data arrival time                                    -6.95
-----------------------------------------------------------
slack (MET)                                           3.01
```

Time Borrowing

In this case, the data path delay is much larger and data becomes available only after the latch closes.

This is clearly a timing violation.



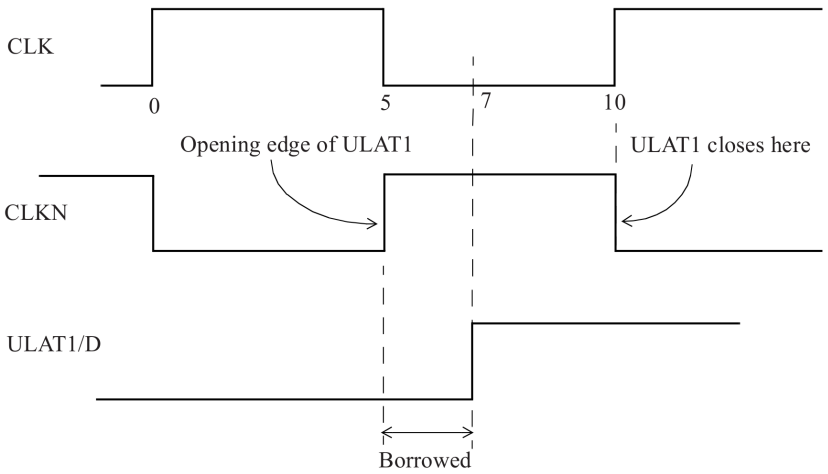
(b) Clock and data waveforms for 7ns data path.

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: ULAT1 (positive level-sensitive latch clocked by CLK')
  Path Group: CLK
  Path Type: max

Point                                                  Incr       Path
-----------------------------------------------------------------------
clock CLK (rise edge)                                  0.00       0.00
clock source latency                                   0.00       0.00
clk (in)                                               0.00       0.00 r
UFF0/CK (DF  )                                         0.00       0.00 r
UFF0/Q (DF  )                                          0.12       0.12 r
UBUF0/Z (BUFF  )                                       6.65       6.77 r
UBUF1/Z (BUFF  )                                       4.33      11.10 r
UBUF2/Z (BUFF  )                                       0.07      11.17 r
ULAT1/D (LH  )                                         0.00      11.17 r
data arrival time                                                11.17
```

Time Borrowing

In this case, the data path delay is much larger and data becomes available only after the latch closes. This is clearly a timing violation.



(b) Clock and data waveforms for 7ns data path.

```
clock CLK' (rise edge)                    5.00       5.00
clock source latency                      0.00       5.00
clk (in)                                  0.00       5.00 f
UINV0/ZN (INV  )                          0.02       5.02 r
ULAT1/G (LH  )                            0.00       5.02 r
time borrowed from endpoint               4.99      10.00
data required time                                  10.00
-----------------------------------------------------------
data required time                                  10.00
data arrival time                                  -11.17
-----------------------------------------------------------
slack (VIOLATED)                                    -1.16

Time Borrowing Information
-----------------------------------------------------------
CLK' nominal pulse width                  5.00
clock latency difference                 -0.00
library setup time                       -0.01
-----------------------------------------------
max time borrow                           4.99
actual time borrow                        4.99
-----------------------------------------------
```

参考书目

- Static Timing Analysis for Nanometer Designs: A Practical Approach. J. Bhasker, Rakesh Chadha. Springer Science Business Media, LLC 2009. Chaper 10.

谢谢聆听！

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