# 数字集成电路静态时序分析基础

邸志雄 博士, zxdi@home.swjtu.edu.cn

西南交通大学信息科学与技术学院

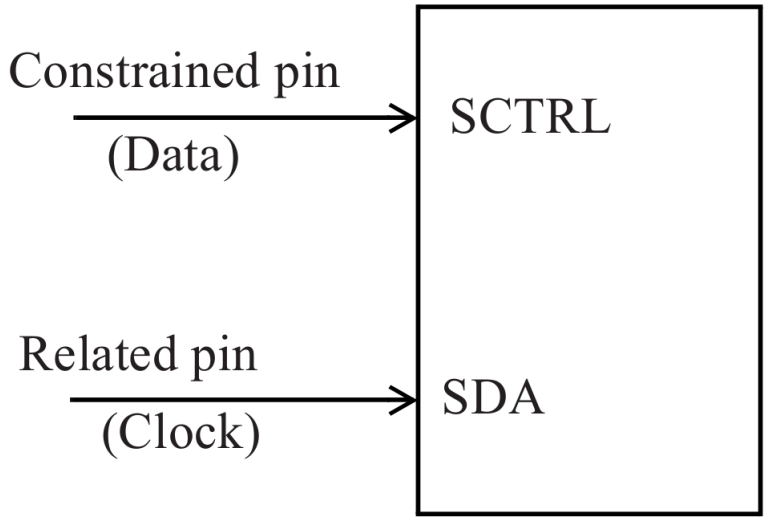
CONTENT

# Part 6: Robust Verification

- Data To Data Checks

## Data To Data Checks

Setup and hold checks can also be applied between any two arbitrary data Pins, neither of which is a clock.




- One pin is the constrained pin, which acts like a data pin of a flip-flop
- The second pin is the related pin, which acts like a clock pin of a flip-flop.

# Data To Data Checks

Distinction with respect to the setup check:

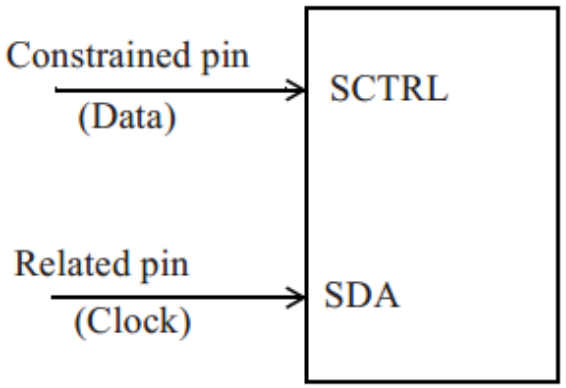
- The data to data setup check is performed on the same edge as the launch edge
- Unlike a normal setup check of a flip-flop, where the capture clock edge is normally one cycle away from the launch clock edge

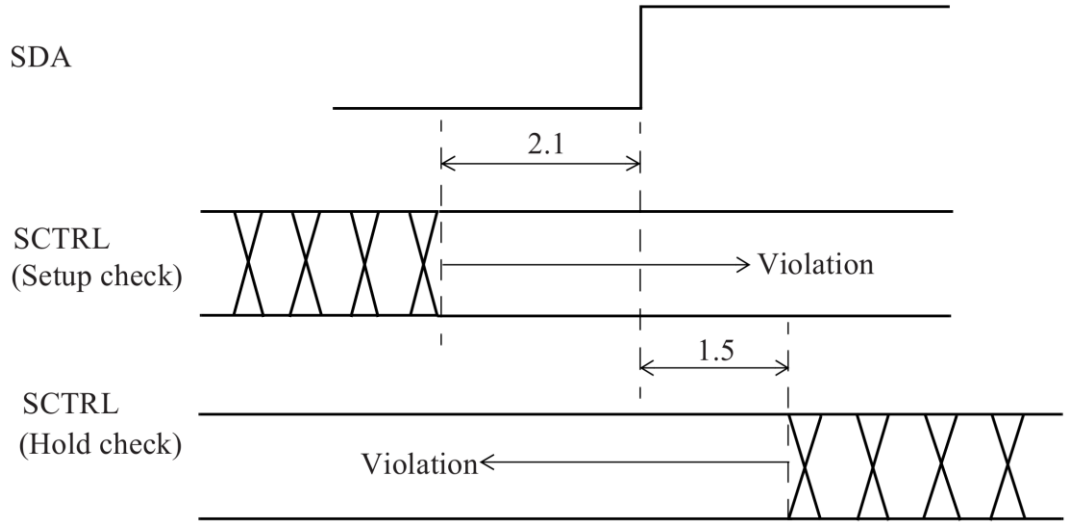
Thus, the data to data setup checks are also referred to as zero-cycle checks or same-cycle checks.

# Data To Data Checks

A data to data check is specified using the set_data_check constraint. Here are example SDC specifications. The data to data setup check is performed on the same edge as the launch edge:

```
set_data_check -from SDA -to SCTRL -setup 2.1
set_data_check -from SDA -to SCTRL -hold 1.5
```



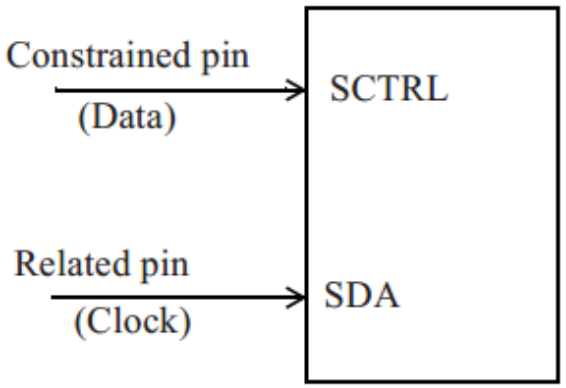



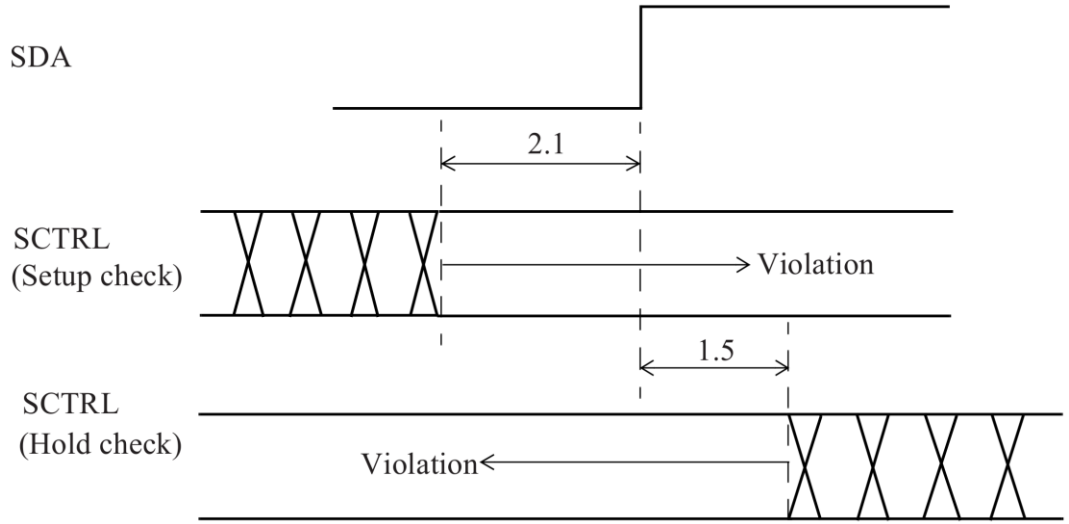

- The setup data check implies that SCTRL should arrive at least 2.1ns prior to the edge of the related pin SDA. Otherwise it is a data to data setup check violation.

# Data To Data Checks

A data to data check is specified using the set_data_check constraint. Here are example SDC specifications. The data to data setup check is performed on the same edge as the launch edge:

```
set_data_check -from SDA -to SCTRL -setup 2.1
set_data_check -from SDA -to SCTRL -hold 1.5
```



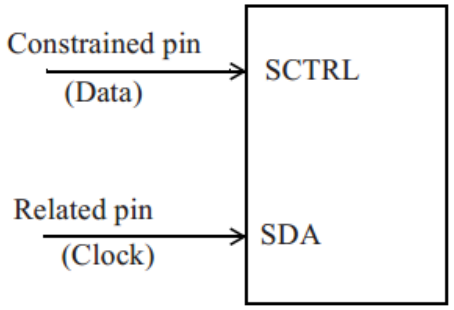



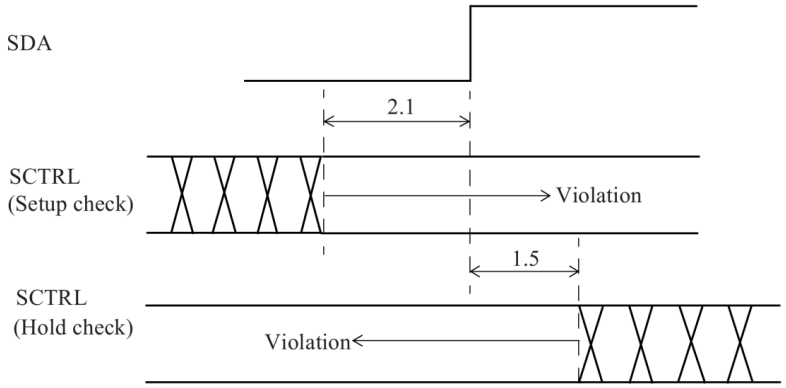

- The hold data check specifies that SCTRL should arrive at least 1.5ns after SDA. If the constrained signal arrives earlier than this specification, then it is a data to data hold check violation

# Data To Data Checks

A data to data check is specified using the set_data_check constraint. Here are example SDC specifications. The data to data setup check is performed on the same edge as the launch edge:

```
set_data_check -from SDA -to SCTRL -setup 2.1
set_data_check -from SDA -to SCTRL -hold 1.5
```




- This check is useful in a custom-designed block where it may be necessary to provide specific arrival times of one signal with respect to another.
- One such common situation is that of a data signal gated by an enable signal and it is required to ensure that the enable signal is stable when the data signal arrives.

# Data To Data Checks

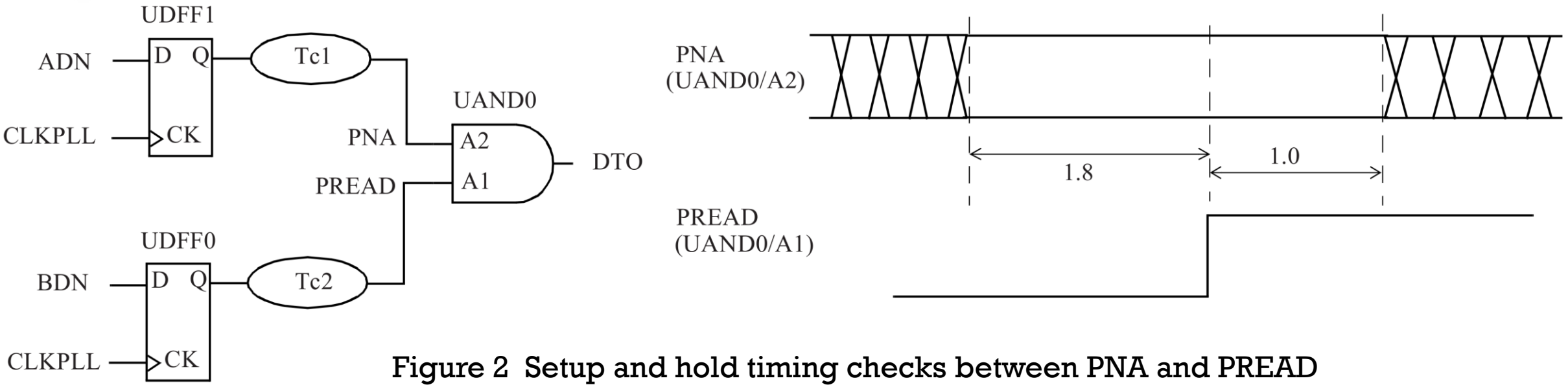



Figure 2 Setup and hold timing checks between PNA and PREAD

Consider the *and* cell shown in Figure 2. The requirement is to ensure that PNA arrives 1.8ns before the rising edge of PREAD and that it should not change for 1.0ns after the rising edge of PREAD. In this example, PNA is the constrained pin and PREAD is the related pin.

Such a requirement can be specified using a data to data setup and hold check:

- set_data_check -from UAND0/A1 -to UAND0/A2 -setup 1.8
- set_data_check -from UAND0/A1 -to UAND0/A2 -hold 1.0

# Data To Data Checks

Here is the setup report.

```
Startpoint: UDFF1
 (rising edge-triggered flip-flop clocked by CLKPLL)
Endpoint: UAND0
 (rising edge-triggered data to data check clocked by CLKPLL)
Path Group: CLKPLL
Path Type: max

Point                                          Incr       Path
-----------------------------------------------------------------
clock CLKPLL (rise edge)                       0.00       0.00
clock source latency                           0.00       0.00
CLKPLL (in)                                    0.00       0.00 r
UDFF1/CK (DF  )                                0.00       0.00 r
UDFF1/Q (DF  )                                 0.12       0.12 f
UBUF0/Z (BUFF  )                               0.06       0.18 f
UAND0/A2 (AN2  )                               0.00       0.18 f
data arrival time                                         0.18

clock CLKPLL (rise edge)                       0.00       0.00
clock source latency                           0.00       0.00
CLKPLL (in)                                    0.00       0.00 r
UDFF0/CK (DF  )                                0.00       0.00 r
UDFF0/Q (DF  )                                 0.12       0.12 r
UBUF1/Z (BUFF  )                               0.05       0.17 r
UBUF2/Z (BUFF  )                               0.05       0.21 r
UBUF3/Z (BUFF  )                               0.05       0.26 r
UAND0/A1 (AN2  )                               0.00       0.26 r
data check setup time                         -1.80      -1.54
data required time                                       -1.54
-----------------------------------------------------------------
data required time                                       -1.54
data arrival time                                        -0.18
-----------------------------------------------------------------
slack (VIOLATED)                                         -1.72
```

The setup time is specified as data check setup time in the report.

The failing report indicates that the PREAD needs to be delayed by at least 1.72ns to ensure that PENA arrives 1.8ns before PREAD - which is our requirement.

# Data To Data Checks

```
Startpoint: UDFF1
 (rising edge-triggered flip-flop clocked by CLKPLL)
Endpoint: UAND0
 (rising edge-triggered data to data check clocked by CLKPLL)
Path Group: CLKPLL
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock CLKPLL (rise edge)                 0.00       0.00
clock source latency                     0.00       0.00
CLKPLL (in)                              0.00       0.00 r
UDFF1/CK (DF  )                          0.00       0.00 r
UDFF1/Q (DF  )                           0.12       0.12 f
UBUF0/Z (BUFF  )                         0.06       0.18 f
UAND0/A2 (AN2  )                         0.00       0.18 f
data arrival time                                   0.18
```

```
clock CLKPLL (rise edge)                 0.00       0.00
clock source latency                     0.00       0.00
CLKPLL (in)                              0.00       0.00 r
UDFF0/CK (DF  )                          0.00       0.00 r
UDFF0/Q (DF  )                           0.12       0.12 r
UBUF1/Z (BUFF  )                         0.05       0.17 r
UBUF2/Z (BUFF  )                         0.05       0.21 r
UBUF3/Z (BUFF  )                         0.05       0.26 r
UAND0/A1 (AN2  )                         0.00       0.26 r
data check setup time                   -1.80      -1.54
data required time                                  -1.54
-----------------------------------------------------------
data required time                                  -1.54
data arrival time                                   -0.18
-----------------------------------------------------------
slack (VIOLATED)                                    -1.72
```

One important aspect of a data to data setup check is that the clock edges that launch both the constrained pin and the related pin are from the same clock cycle (also referred to as same-cycle checks).

Thus notice in the report that the starting time for the capture edge (UDFF0/CK) is at 0ns, not one cycle later as one would typically see in a setup report.

# Data To Data Checks

The zero-cycle setup check causes the hold timing check to be different from other hold check reports - the hold check is no longer on the same clock edge.

Here is the clock specification for CLKPLL which is utilized for the hold path report below.

create_clock -name CLKPLL -period 10 -waveform {0 5} [get_ports CLKPLL]

```
Startpoint: UDFF1
  (rising edge-triggered flip-flop clocked by CLKPLL)
Endpoint: UAND0
  (falling edge-triggered data to data check clocked by CLKPLL)
Path Group: CLKPLL
Path Type: min

Point                                   Incr       Path
-----------------------------------------------------------
clock CLKPLL (rise edge)               10.00      10.00
clock source latency                    0.00      10.00
CLKPLL (in)                             0.00      10.00 r
UDFF1/CK (DF  )                         0.00      10.00 r
UDFF1/Q (DF  ) <-                       0.12      10.12 r
UBUF0/Z (BUFF  )                        0.05      10.17 r
UAND0/A2 (AN2  )                        0.00      10.17 r
data arrival time                                 10.17

clock CLKPLL (rise edge)                0.00       0.00
clock source latency                    0.00       0.00
CLKPLL (in)                             0.00       0.00 r
UDFF0/CK (DF  )                         0.00       0.00 r
UDFF0/Q (DF  )                          0.12       0.12 f
UBUF1/Z (BUFF  )                        0.06       0.18 f
UBUF2/Z (BUFF  )                        0.05       0.23 f
UBUF3/Z (BUFF  )                        0.06       0.29 f
UAND0/A1 (AN2  )                        0.00       0.29 f
data check hold time                    1.00       1.29
data required time                                 1.29
-----------------------------------------------------------
data required time                                 1.29
data arrival time                                -10.17
-----------------------------------------------------------
slack (MET)                                        8.88
```

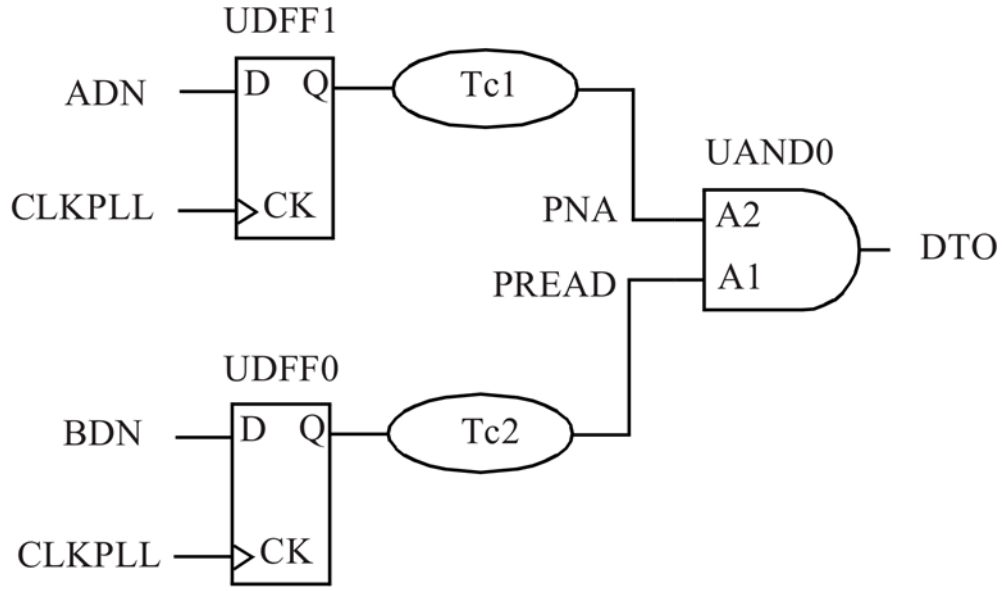
# Data To Data Checks

In some scenarios, a designer may require the data to data hold check to be performed on the same clock cycle.

The same cycle hold requirement implies that the clock edge used for the related pin be moved back to where the clock edge for the constrained pin is.

This can be achieved by specifying a multicycle of -1 :

- set_multicycle_path -1 -hold -to UAND0/A2



# Data To Data Checks

Here is the hold timing report for the example above with this multicycle specification.

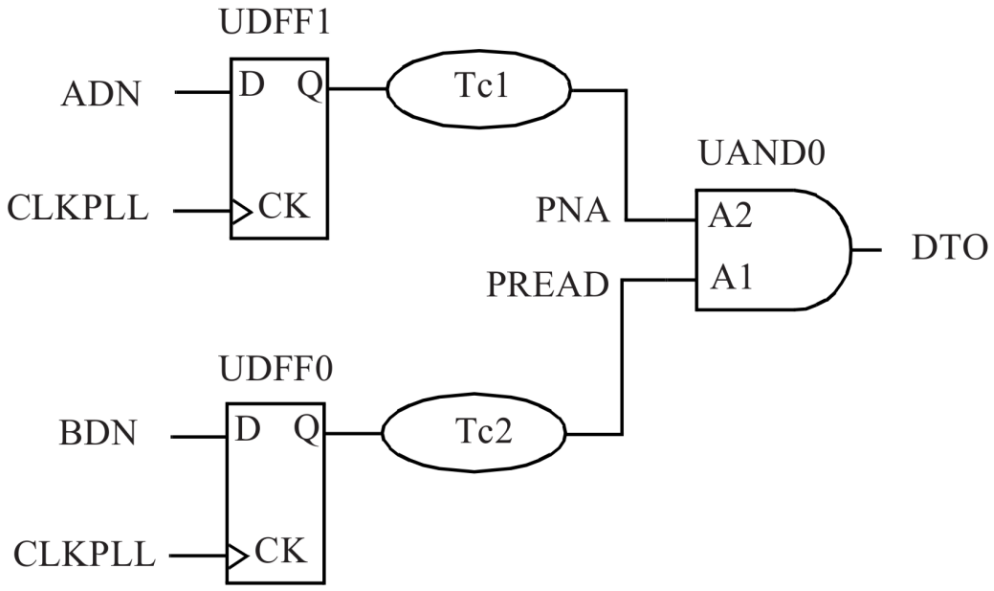
```
Startpoint: UDFF1
  (rising edge-triggered flip-flop clocked by CLKPLL)
Endpoint: UAND0
  (falling edge-triggered data to data check clocked by CLKPLL)
Path Group: CLKPLL
Path Type: min

Point                                    Incr       Path
-----------------------------------------------------------
clock CLKPLL (rise edge)                 0.00       0.00
clock source latency                     0.00       0.00
CLKPLL (in)                              0.00       0.00 r
UDFF1/CK (DF   )                         0.00       0.00 r
UDFF1/Q (DF   ) <-                       0.12       0.12 r
UBUF0/Z (BUFF   )                        0.05       0.17 r
UAND0/A2 (AN2   )                        0.00       0.17 r
data arrival time                                   0.17

clock CLKPLL (rise edge)                 0.00       0.00
clock source latency                     0.00       0.00
CLKPLL (in)                              0.00       0.00 r
UDFF0/CK (DF   )                         0.00       0.00 r
UDFF0/Q (DF   )                          0.12       0.12 f
UBUF1/Z (BUFF   )                        0.06       0.18 f
UBUF2/Z (BUFF   )                        0.05       0.23 f
UBUF3/Z (BUFF   )                        0.06       0.29 f
UAND0/A1 (AN2   )                        0.00       0.29 f
data check hold time                     1.00       1.29
data required time                                  1.29
-----------------------------------------------------------
data required time                                  1.29
data arrival time                                  -0.17
-----------------------------------------------------------
slack (VIOLATED)                                   -1.12
```

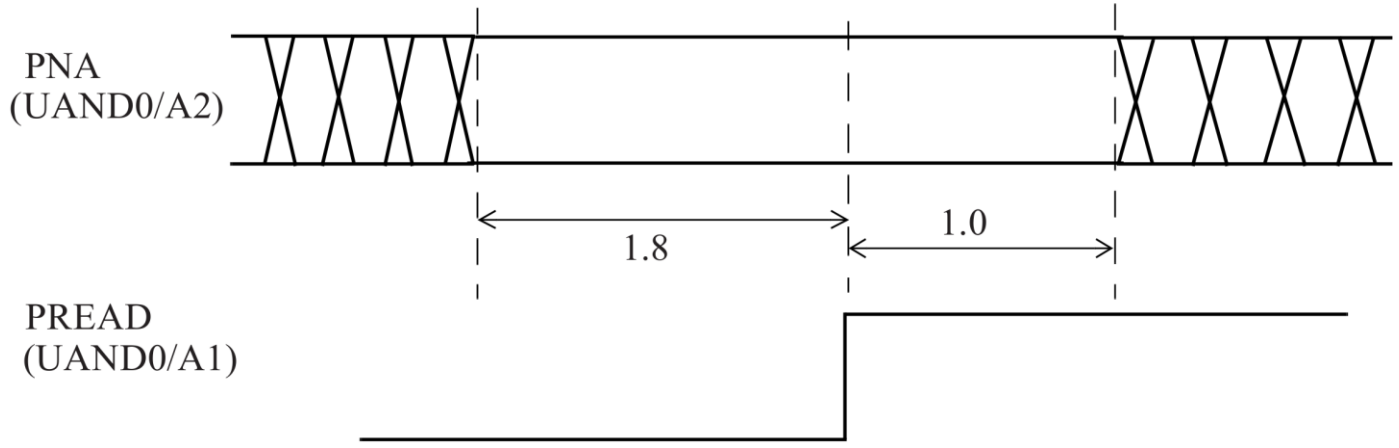
The hold check is now performed using the same clock edge for the constrained pin and the related pin.

# Data To Data Checks

An alternate way of having the data to data hold check performed in the same cycle is to specify this as a data to data setup check between the pins in the reverse direction.

- set_data_check -from UAND0/A2 -to UAND0/A1 -setup 1.0




- set_data_check -from UAND0/A1 -to UAND0/A2 -setup 1.8
- set_data_check -from UAND0/A1 -to UAND0/A2 -hold 1.0

# Data To Data Checks

- The data to data check is also useful in defining a no-change data check.
- This is done by specifying a setup check on the rising edge and a hold check on the falling edge, such that a no-change window gets effectively defined.

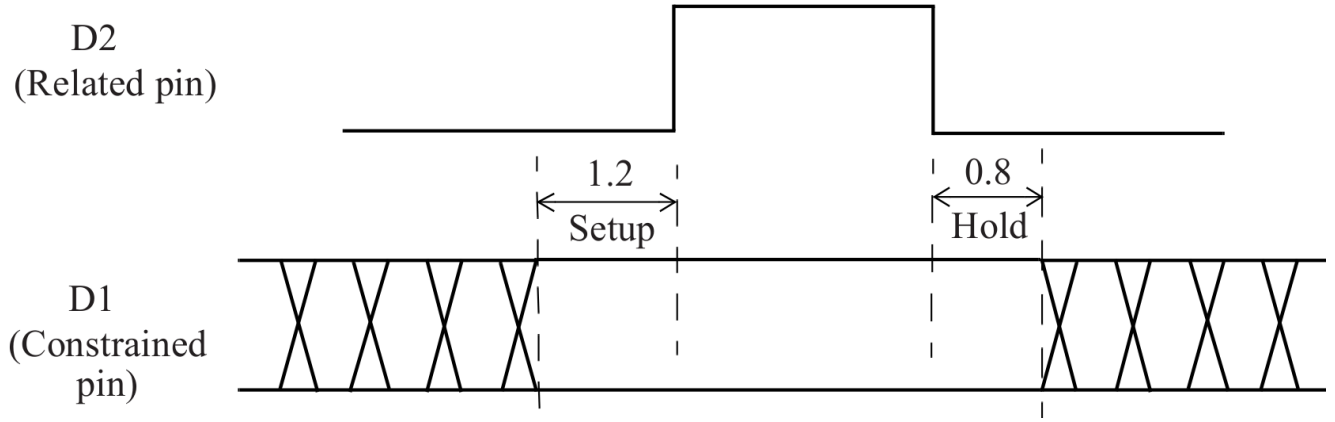



Figure 3 A no-change data check achieved using setup and hold data checks

Here are the specifications for this scenario:

- set_data_check -rise_from D2 -to D1 -setup 1.2
- set_data_check -fall_from D2 -to D1 -hold 0.8

# 参考书目

- Static Timing Analysis for Nanometer Designs: A Practical Approach. J. Bhasker, Rakesh Chadha. Springer Science Business Media, LLC 2009. Chaper 10.

# 谢谢聆听！

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