数字集成电路静态时序分析基础

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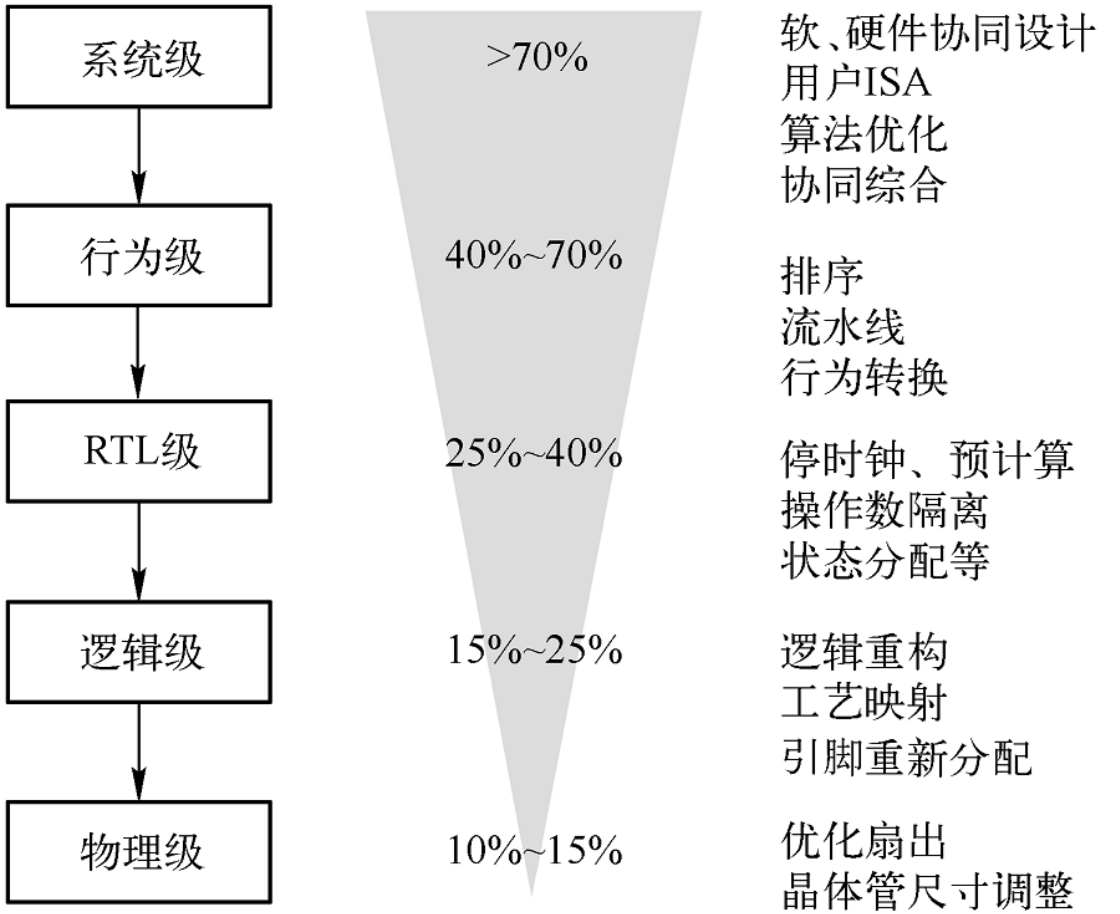
CONTENT

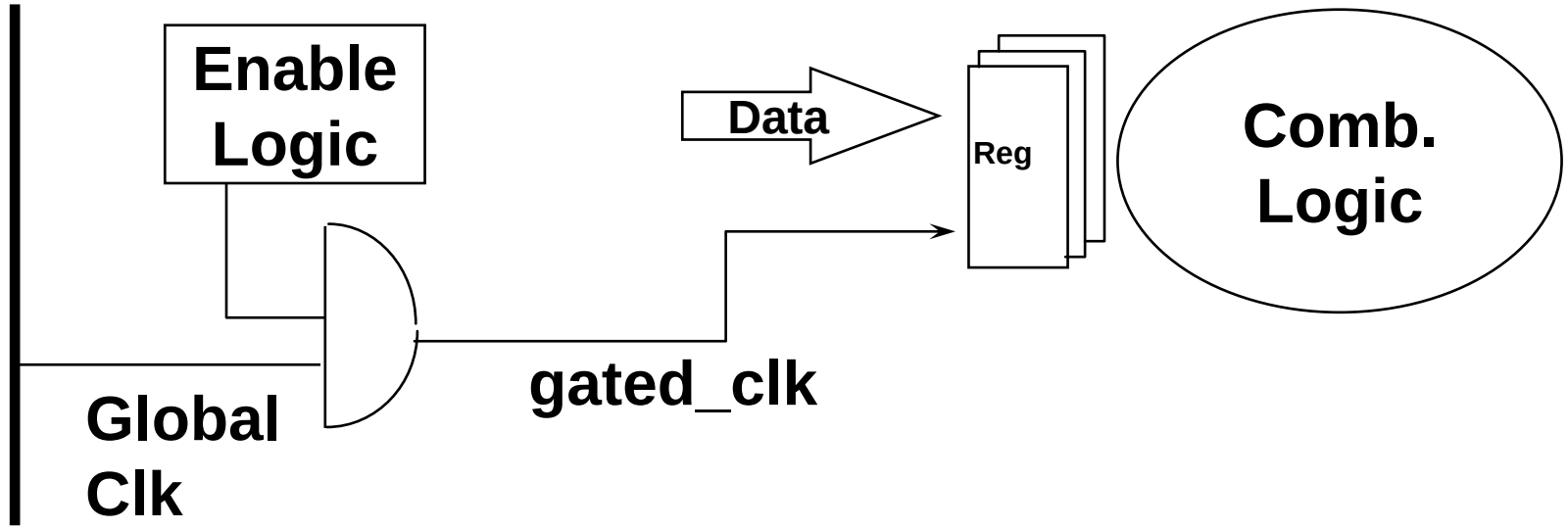
Part 6: Clock Gating Checks

Clock Gating



[引用自:SoC设计与实现（第3版），郭炜 著.电子工业出版社.]

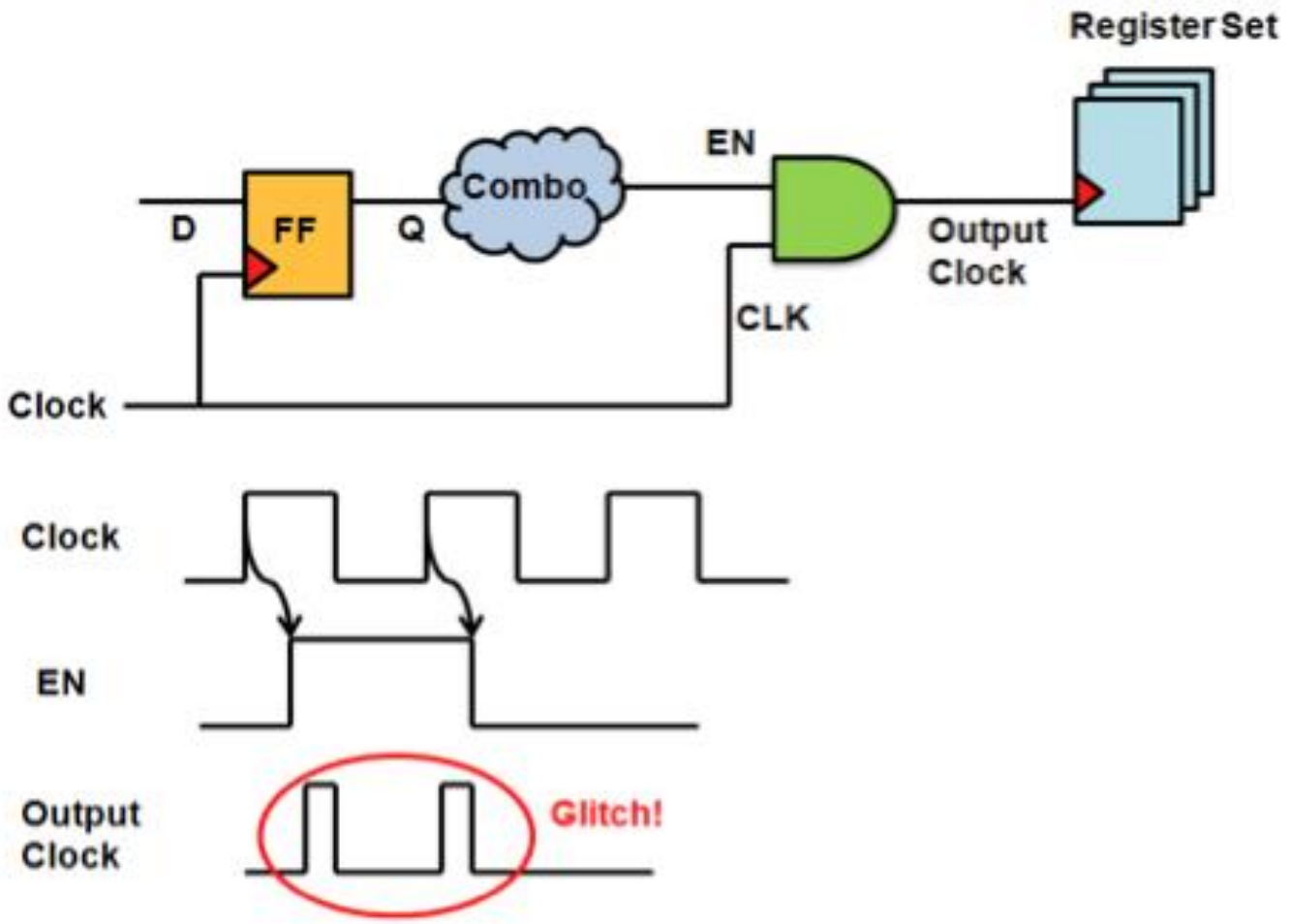
Clock Gating



- Toggling consume power.
- Enable the module clock only when needed

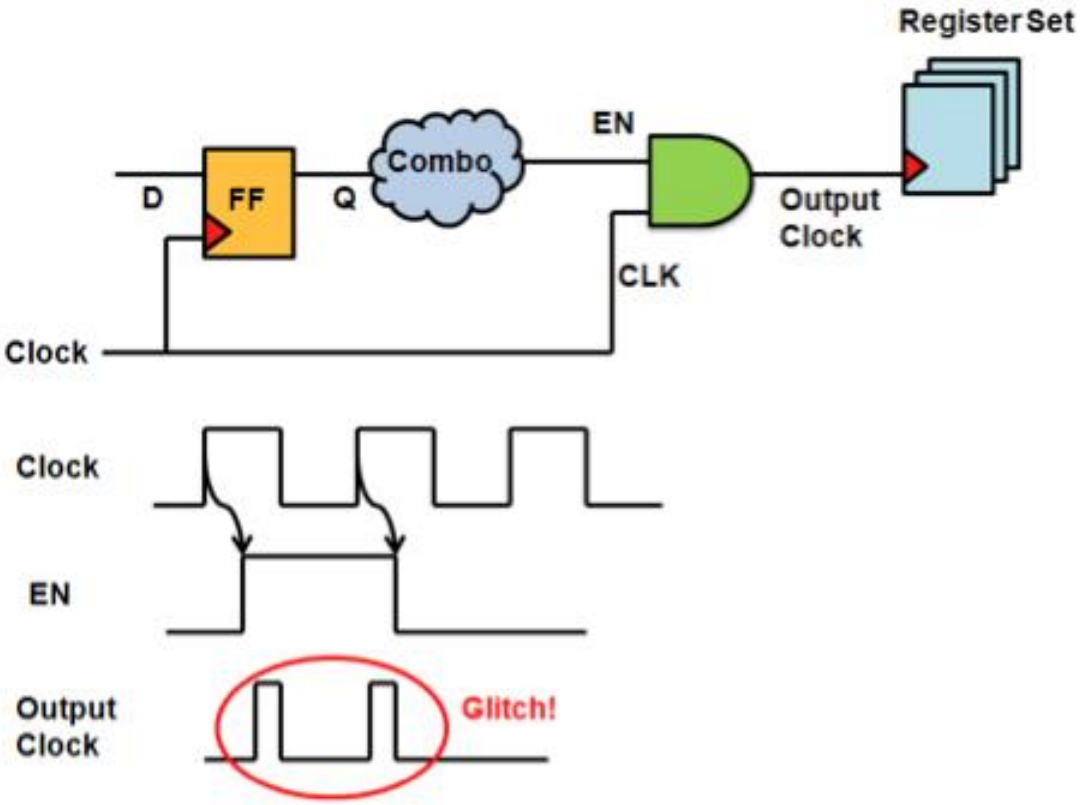
[引用自: SoC设计与实现（第3版），郭炜 著. 电子工业出版社.]

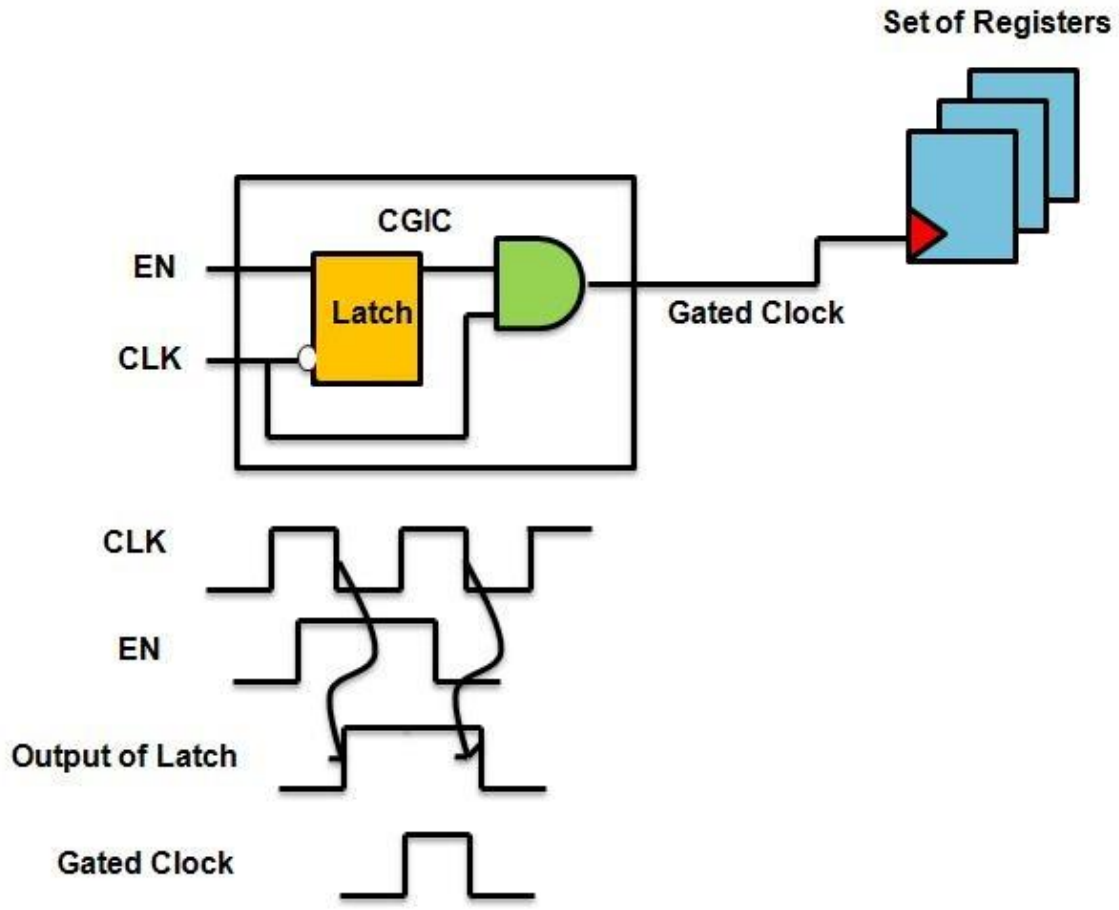
Clock Gating



[引用自http://vlsi-soc.blogspot.com/2012/08/clock-gating-integrated-cell.html]

Clock Gating





Clock gating cells and a glitch free clock gating

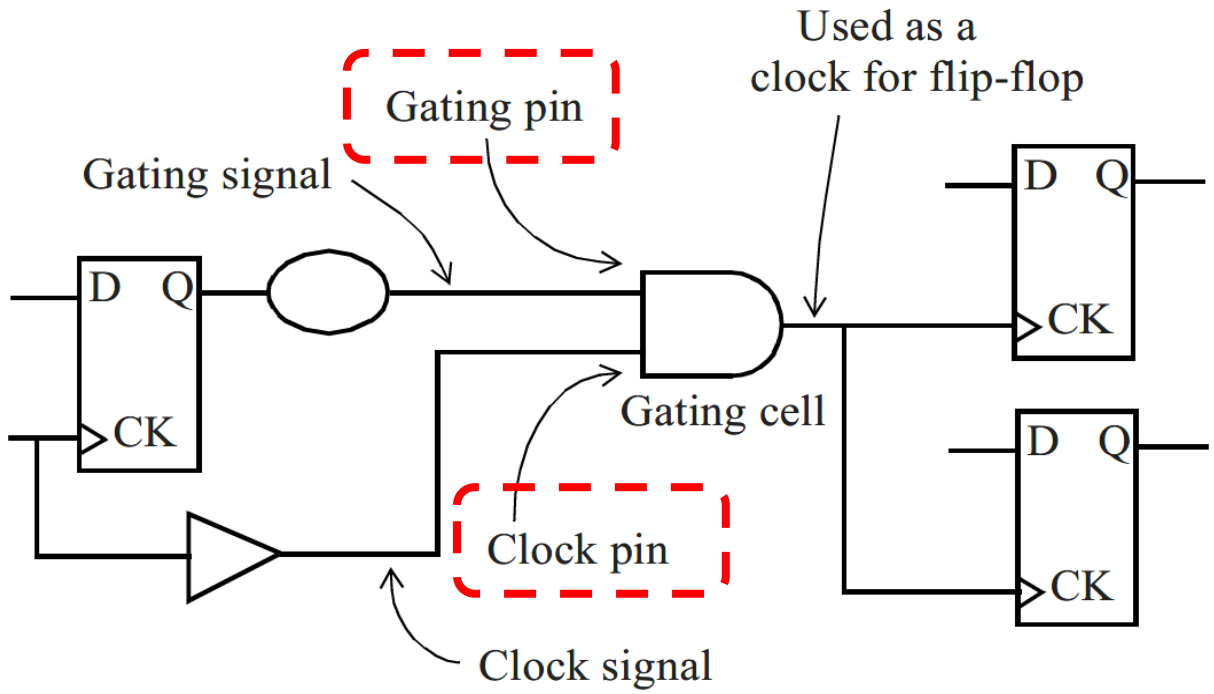
[引用自http://vlsi-soc.blogspot.com/2012/08/clock-gating-integrated-cell.html]

Clock Gating Checks

A clock gating check occurs when a gating signal can control the path of a clock signal at a logic cell.

Conditions for a clock gating check:

- The clock that goes through the cell must be used as a clock downstream. If the clock is not used as a clock after the gating cell, then no clock gating check is inferred.
- Another condition for the clock gating check applies to the gating signal. The signal at the gating pin of the check should not be a clock or if it is a clock, it should not be used as a clock downstream



Clock Gating Checks

Consider the example in Figure 2.

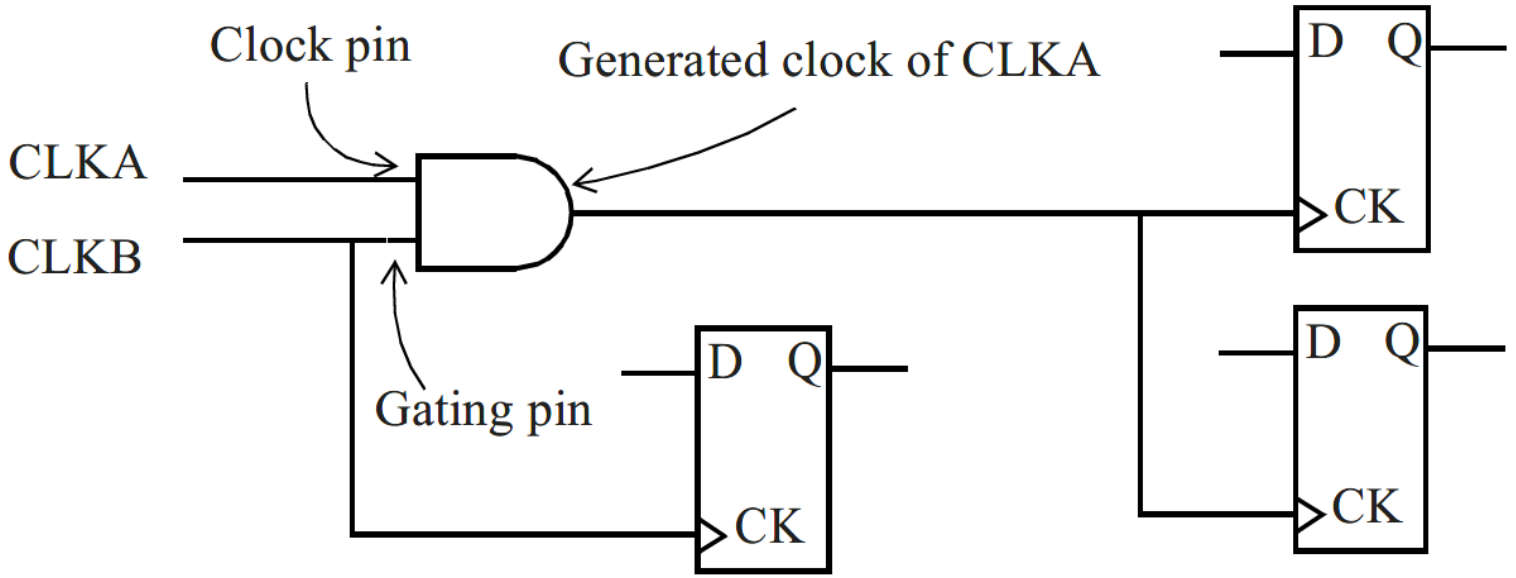


Figure 2 Gating check inferred - clock at the gating pin not used as a clock downstream.

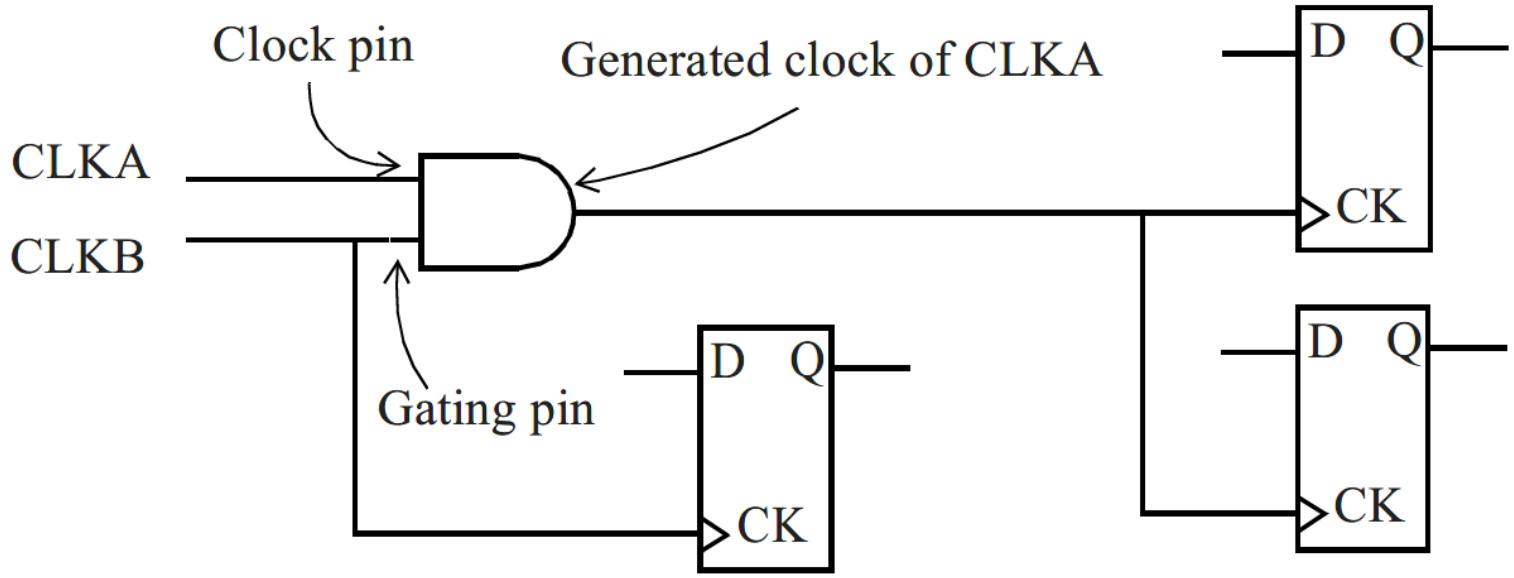
CLKB is not used as a clock downstream due to the definition of the generated clock of CLKA- the path of CLKB is blocked by the generated clock definition.

Clock Gating Checks

There are two types of clock gating checks inferred:

- Active-high clock gating check: Occurs when the gating cell has an *and* or a *nand* function.
- Active-low clock gating check: Occurs when the gating cell has an ***or*** or a ***nor*** function.

The active-high and active-low refer to the logic state of the gating signal which **activates** the clock signal at the output of the gating cell.



Clock Gating Checks

If the gating cell is a complex function where the gating relationship is not obvious, such as a *multiplexer* or an *xor* cell, STA output will typically provide a warning that no clock gating check is being inferred.

However this can be changed by specifying a clock gating relationship for the gating cell explicitly by using the command : *set_clock_gating_check.*

Clock Gating Checks---Active-High Clock Gating

Active-High Clock Gating occurs at an *and* or a *nand* cell

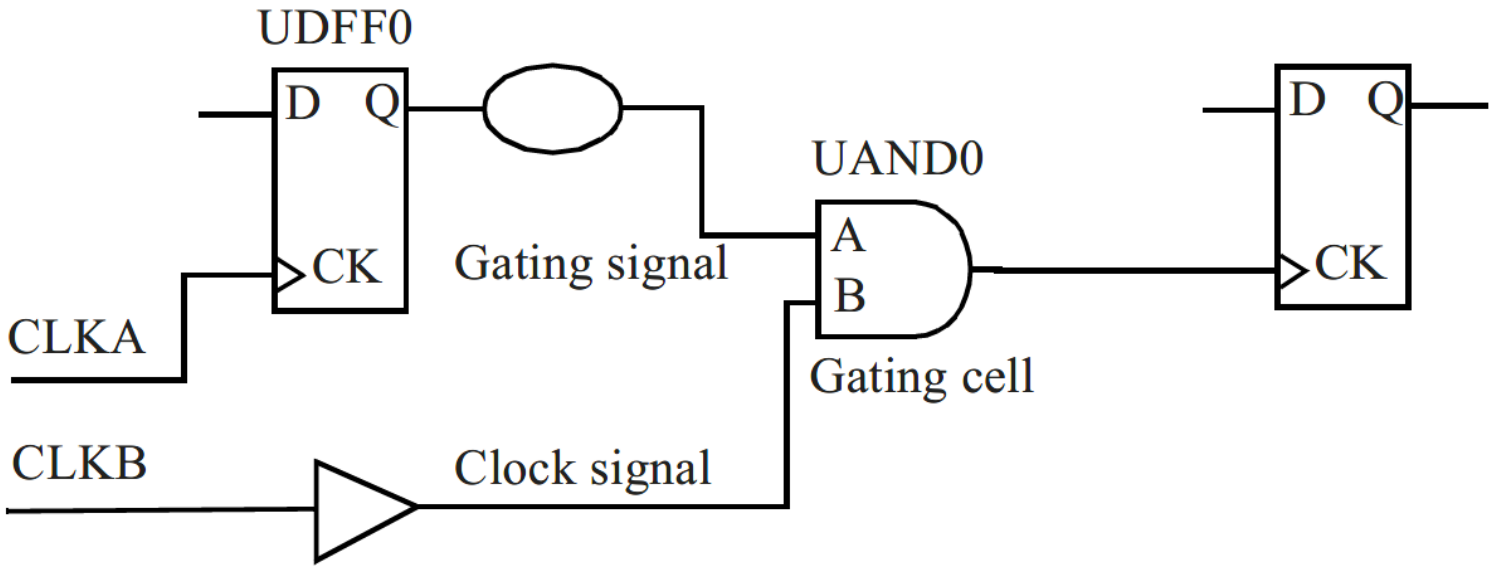


Figure 3 Active high clock gating using an AND cell.

- Pin B of the gating cell is the clock signal
- Pin A of the gating cell is the gating signal

Clock Gating Checks---Active-High Clock Gating

Assume that both clocks CLKA and CLKB have the same waveforms.

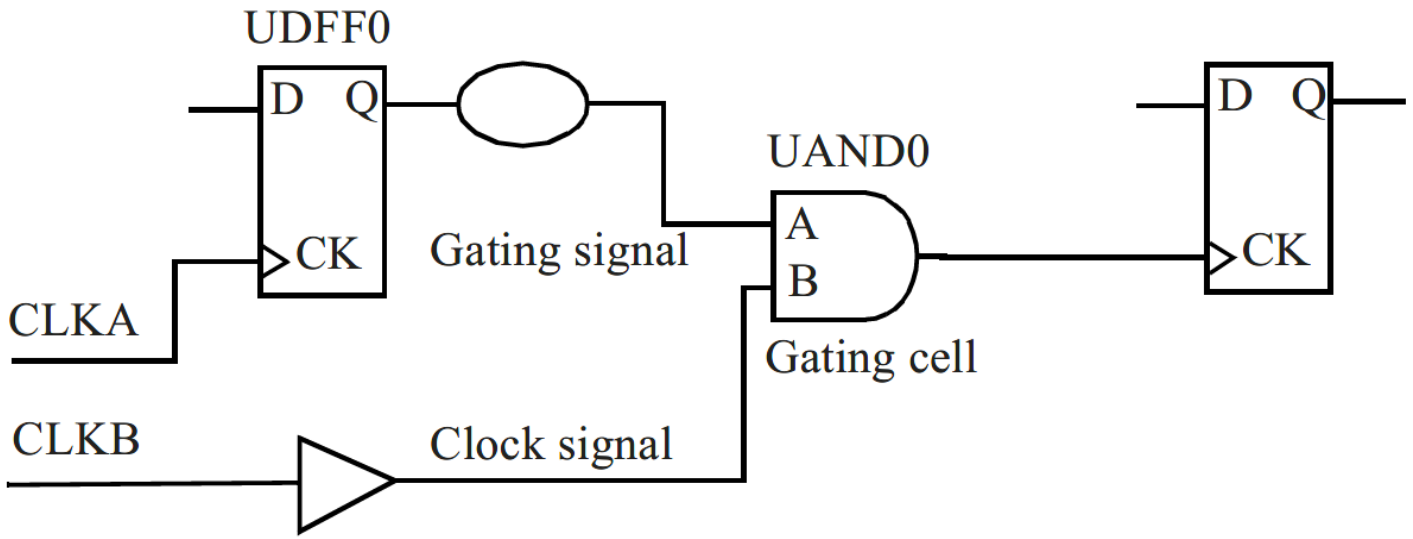
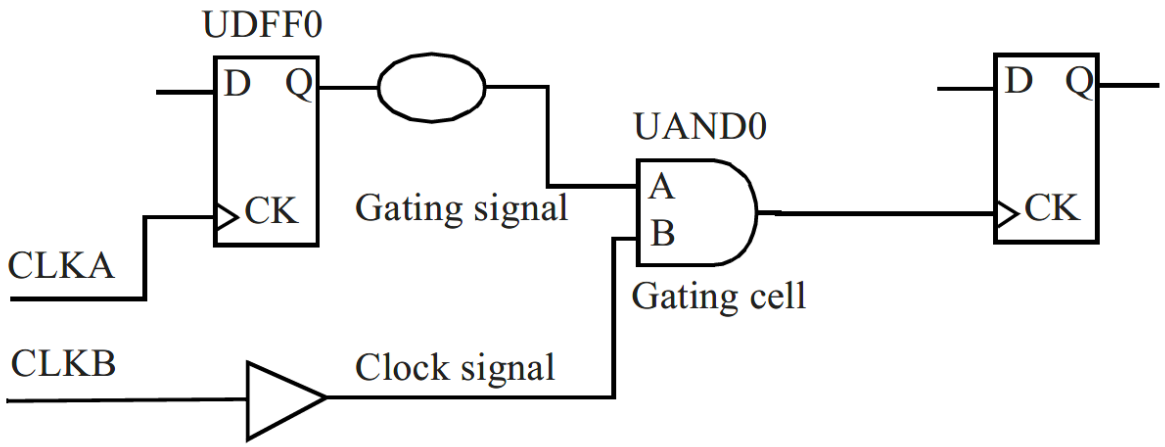


Figure 3 Active high clock gating using an AND cell.

create_clock -name CLKA -period 10 -waveform {0 5} [get_ports CLKA]

create_clock -name CLKB -period 10 -waveform {0 5} [get_ports CLKB]

Clock Gating Checks---Active-High Clock Gating



- The active-high clock gating setup check requires that the gating signal changes before the clock goes high.
- The active-high clock gating hold check requires that the gating signal changes only after the falling edge of the clock.

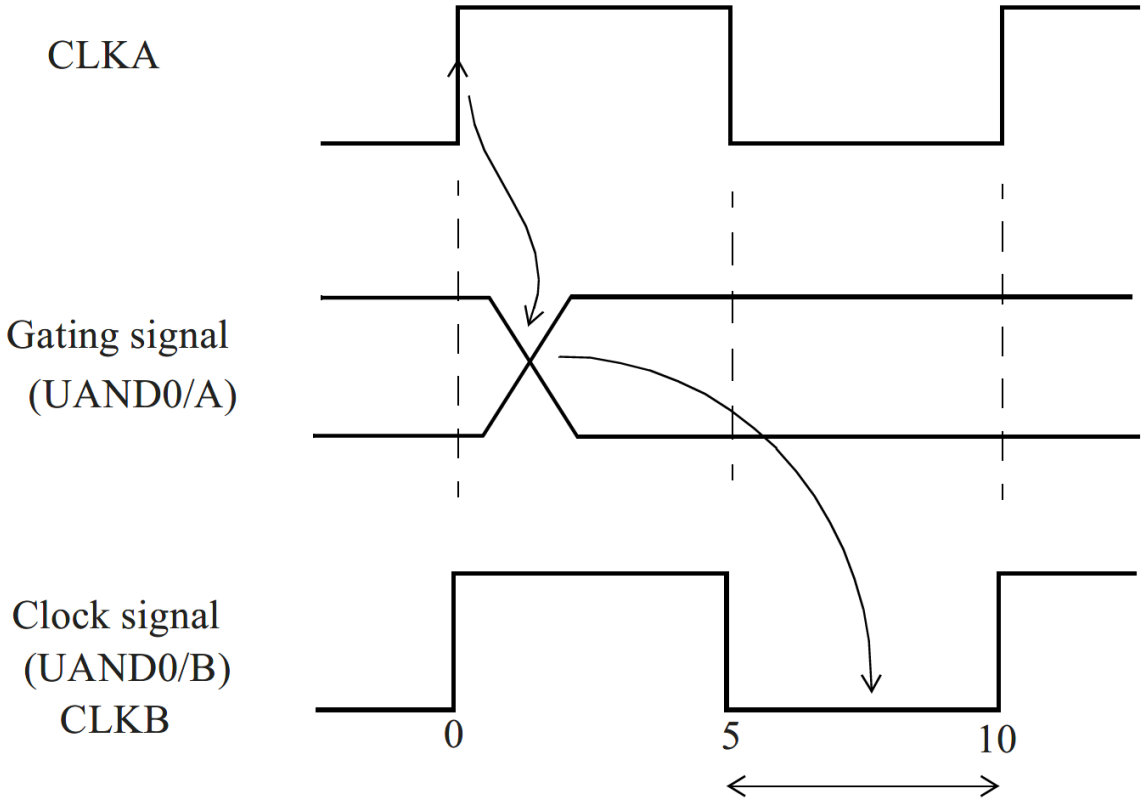


Figure 4 Gating signal needs to be delayed.

Clock Gating Checks---Active-High Clock Gating

Here is the setup path report.

```
Startpoint: UDFF0
  (rising edge-triggered flip-flop clocked by CLKA)
Endpoint: UAND0
  (rising clock gating-check end-point clocked by CLKB)
Path Group: **clock_gating_default**
Path Type: max

Point                                          Incr       Path
-----------------------------------------------------------------
clock CLKA (rise edge)                         0.00       0.00
clock source latency                           0.00       0.00
CLKA (in)                                      0.00       0.00 r
UDFF0/CK (DF   )                               0.00       0.00 r
UDFF0/Q (DF   )                                0.13       0.13 f
UAND0/A1 (AN2   )                              0.00       0.13 f
data arrival time                                         0.13
```

Clock Gating Checks---Active-High Clock Gating

```
clock CLKB (rise edge)                    10.00       10.00
clock source latency                       0.00       10.00
CLKB (in)                                  0.00       10.00 r
UAND0/A2 (AN2  )                           0.00       10.00 r
clock gating setup time                    0.00       10.00
data required time                                    10.00
-------------------------------------------------------------
data required time                                    10.00
data arrival time                                     -0.13
-------------------------------------------------------------
slack (MET)                                            9.87
```

- The check validates that the gating signal changes before the next rising edge of clock CLKB at 10ns.

Clock Gating Checks---Active-High Clock Gating

The active-high clock gating hold check requires that the gating signal changes only after the falling edge of the clock. Here is the hold path report.

```
Startpoint: UDFF0
  (rising edge-triggered flip-flop clocked by CLKA)
Endpoint: UAND0
  (rising clock gating-check end-point clocked by CLKB)
Path Group: **clock_gating_default**
Path Type: min

Point                                          Incr       Path
-----------------------------------------------------------------
clock CLKA (rise edge)                         0.00       0.00
clock source latency                           0.00       0.00
CLKA (in)                                      0.00       0.00 r
UDFF0/CK (DF  )                                0.00       0.00 r
UDFF0/Q (DF  )                                 0.13       0.13 r
UAND0/A1 (AN2  )                               0.00       0.13 r
data arrival time                                         0.13
```

Clock Gating Checks---Active-High Clock Gating

```
clock CLKB (fall edge)                    5.00        5.00
clock source latency                      0.00        5.00
CLKB (in)                                 0.00        5.00 f
UAND0/A2 (AN2  )                          0.00        5.00 f
clock gating hold time                    0.00        5.00
data required time                                    5.00
-------------------------------------------------------------
data required time                                    5.00
data arrival time                                    -0.13
-------------------------------------------------------------
slack (VIOLATED)                                     -4.87
```

The hold gating check fails because the gating signal is changing too fast, before the falling edge of CLKB at 5ns.

One can see that the hold time requirement is quite large. This is caused by the fact that the sense of the gating signal and the flip-flops being gated are the same.

Clock Gating Checks---Active-High Clock Gating

This can be resolved by using a different type of launch flip-flop, say, a negative edge-triggered flip-flop to generate the gating signal. Such an example is shown next.

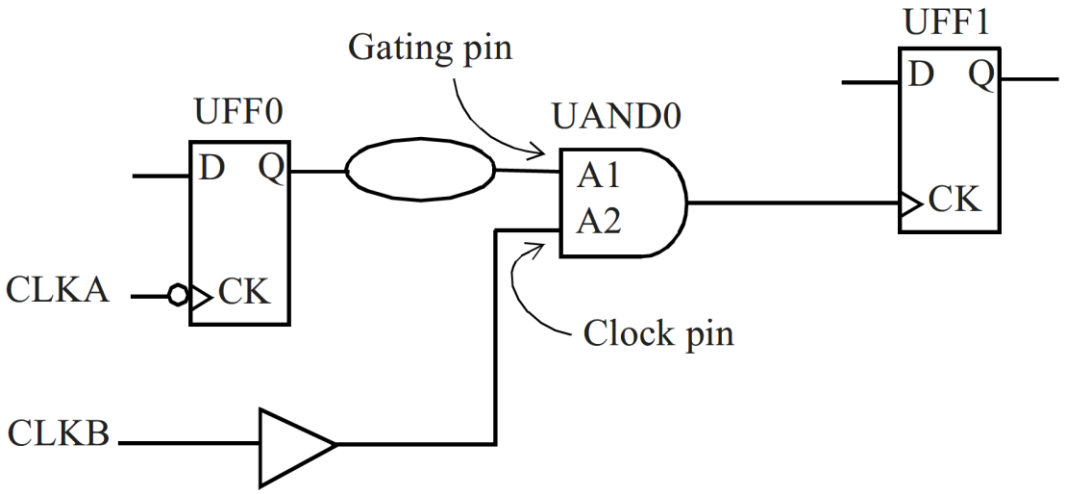
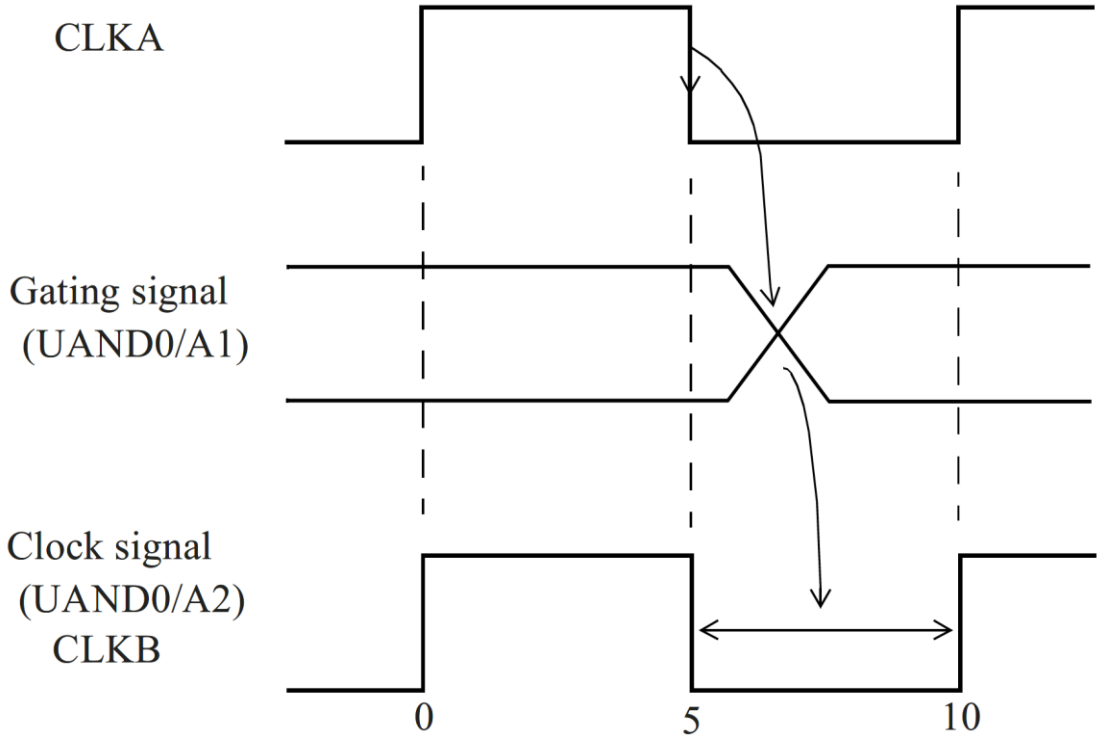


Figure 5 Gating signal clocked on falling edge.



Safe clock gating implies that the output of flip-flop UFF0 **must** change during the inactive part of the gating clock, which is between 5ns and 10ns.

Clock Gating Checks---Active-High Clock Gating

Here is the setup path report.

```
Path Group: **clock_gating_default**
Path Type: max

Point                                          Incr       Path
-----------------------------------------------------------------
clock CLKA (fall edge)                         5.00       5.00
clock source latency                           0.00       5.00
CLKA (in)                                      0.00       5.00 f
UFF0/CKN (DFN  )                               0.00       5.00 f
UFF0/Q (DFN  )                                 0.15       5.15 r
UAND0/A1 (AN2  )                               0.00       5.15 r
data arrival time                                         5.15
```

Clock Gating Checks---Active-High Clock Gating

```
clock CLKB (rise edge)                    10.00       10.00
clock source latency                       0.00       10.00
CLKB (in)                                  0.00       10.00 r
UAND0/A2 (AN2  )                           0.00       10.00 r
clock gating setup time                    0.00       10.00
data required time                                    10.00
-----------------------------------------------------------

data required time                                    10.00

data arrival time                                     -5.15
-----------------------------------------------------------

slack (MET)                                            4.85
```

Clock Gating Checks---Active-High Clock Gating

Here is the clock gating hold report. Notice that the hold time check is much easier to meet with the new design.

```
Startpoint: UFF0
  (falling edge-triggered flip-flop clocked by CLKA)
Endpoint: UAND0
  (rising clock gating-check end-point clocked by CLKB)
Path Group: **clock_gating_default**
Path Type: min

Point                                          Incr       Path
-----------------------------------------------------------------
clock CLKA (fall edge)                         5.00       5.00
clock source latency                           0.00       5.00
CLKA (in)                                      0.00       5.00 f
UFF0/CKN (DFN  )                               0.00       5.00 f
UFF0/Q (DFN  )                                 0.13       5.13 f
UAND0/A1 (AN2  )                               0.00       5.13 f
data arrival time                                         5.13
```

Clock Gating Checks---Active-High Clock Gating

```
clock CLKB (fall edge)                  5.00        5.00
clock source latency                    0.00        5.00
CLKB (in)                               0.00        5.00 f
UAND0/A2 (AN2  )                        0.00        5.00 f
clock gating hold time                  0.00        5.00
data required time                                  5.00
-------------------------------------------------------------
data required time                                  5.00
data arrival time                                  -5.13
-------------------------------------------------------------
slack (MET)                                         0.13
```

Since the clock edge (negative edge) that launches the gating signal is opposite of the clock being gated (active-high), the setup and hold requirements are easy to meet.

This is the most common structure used for gated clocks.

Clock Gating Checks---Active-Low Clock Gating

Figure 7 shows an example of an active-low clock gating check.

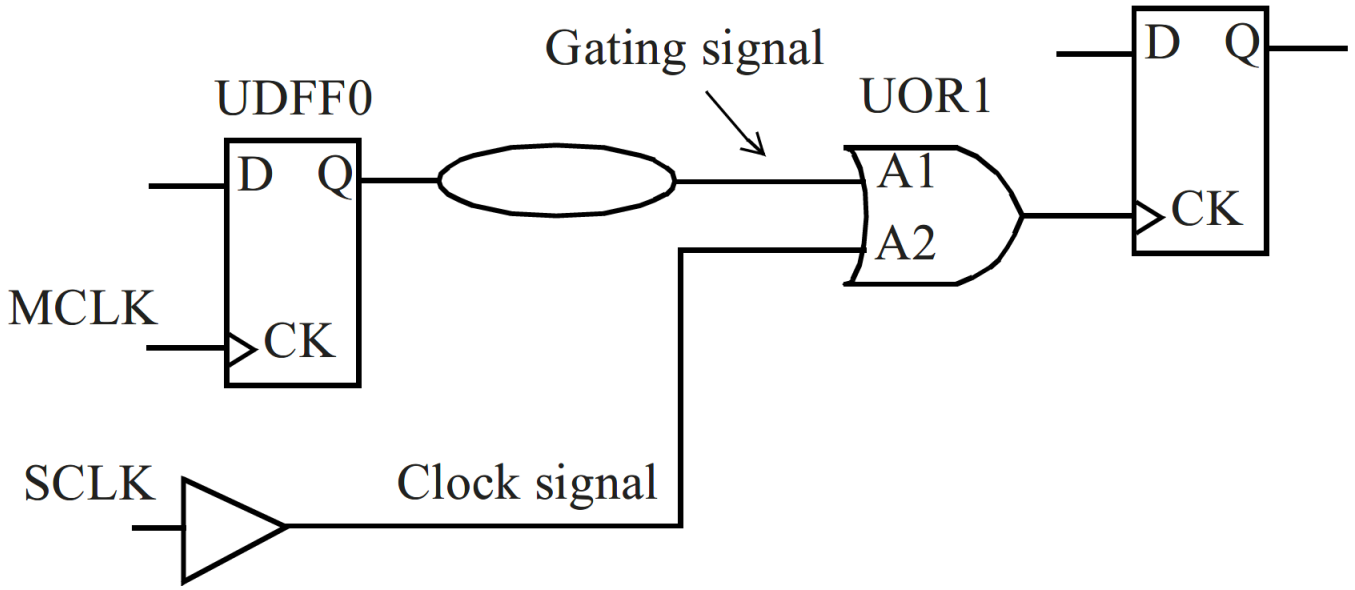


Figure 7 Active-low clock gating check.

create_clock -name MCLK -period 8 -waveform {0 4} [get_ports MCLK]

create_clock -name SCLK -period 8 -waveform {0 4} [get_ports SCLK]

Clock Gating Checks---Active-Low Clock Gating

The gating signal should switch only when the clock is high as illustrated in Figure 8

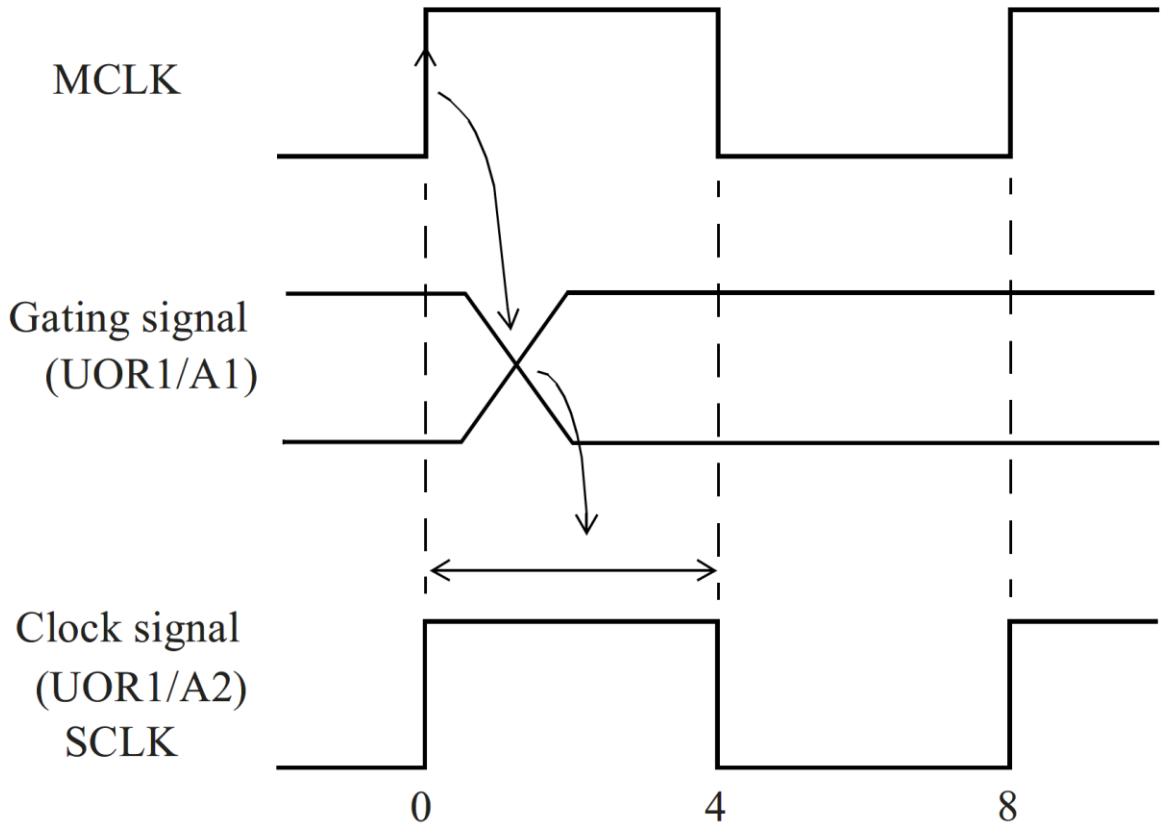


Figure 8 Gating signal changes when clock is high

Clock Gating Checks---Active-Low Clock Gating

Here is the active-low clock gating setup timing report.

```
Startpoint: UDFF0
  (rising edge-triggered flip-flop clocked by MCLK)
Endpoint: UOR1
  (falling clock gating-check end-point clocked by SCLK)
Path Group: **clock_gating_default**
Path Type: max

Point                                          Incr       Path
-----------------------------------------------------------------
clock MCLK (rise edge)                         0.00       0.00
clock source latency                           0.00       0.00
MCLK (in)                                      0.00       0.00 r
UDFF0/CK (DF  )                                0.00       0.00 r
UDFF0/Q (DF  )                                 0.13       0.13 f
UOR1/A1 (OR2  )                                0.00       0.13 f
data arrival time                                         0.13
```

Clock Gating Checks---Active-Low Clock Gating

```
clock SCLK (fall edge)                    4.00       4.00
clock source latency                      0.00       4.00
SCLK (in)                                 0.00       4.00 f
UOR1/A2 (OR2  )                           0.00       4.00 f
clock gating setup time                   0.00       4.00

data required time                                   4.00
-----------------------------------------------------------
data required time                                   4.00
data arrival time                                   -0.13
-----------------------------------------------------------
slack (MET)                                          3.87
```

This check ensures that the gating signal arrives before the clock edge becomes inactive, in this case, at 4ns.

Clock Gating Checks---Active-Low Clock Gating

Here is the clock gating hold timing report.

```
Startpoint: UDFF0
  (rising edge-triggered flip-flop clocked by MCLK)
Endpoint: UOR1
  (falling clock gating-check end-point clocked by SCLK)
Path Group: **clock_gating_default**
Path Type: min

Point                                          Incr       Path
-----------------------------------------------------------------
clock MCLK (rise edge)                         0.00       0.00
clock source latency                           0.00       0.00
MCLK (in)                                      0.00       0.00 r
UDFF0/CK (DF  )                                0.00       0.00 r
UDFF0/Q (DF  )                                 0.13       0.13 r
UOR1/A1 (OR2  )                                0.00       0.13 r
data arrival time                                         0.13
```

Clock Gating Checks---Active-Low Clock Gating

```
clock SCLK (rise edge)                    0.00        0.00
clock source latency                      0.00        0.00
SCLK (in)                                 0.00        0.00 r
UOR1/A2 (OR2  )                           0.00        0.00 r
clock gating hold time                    0.00        0.00
data required time                                    0.00
-------------------------------------------------------------
data required time                                    0.00
data arrival time                                    -0.13
-------------------------------------------------------------
slack (MET)                                           0.13
```

This check ensures that the gating signal changes only after the rising edge of the clock signal, which in this case is at 0ns.

Clock Gating Checks---Clock Gating with a Multiplexer

Figure 9 shows an example of clock gating using a multiplexer cell.

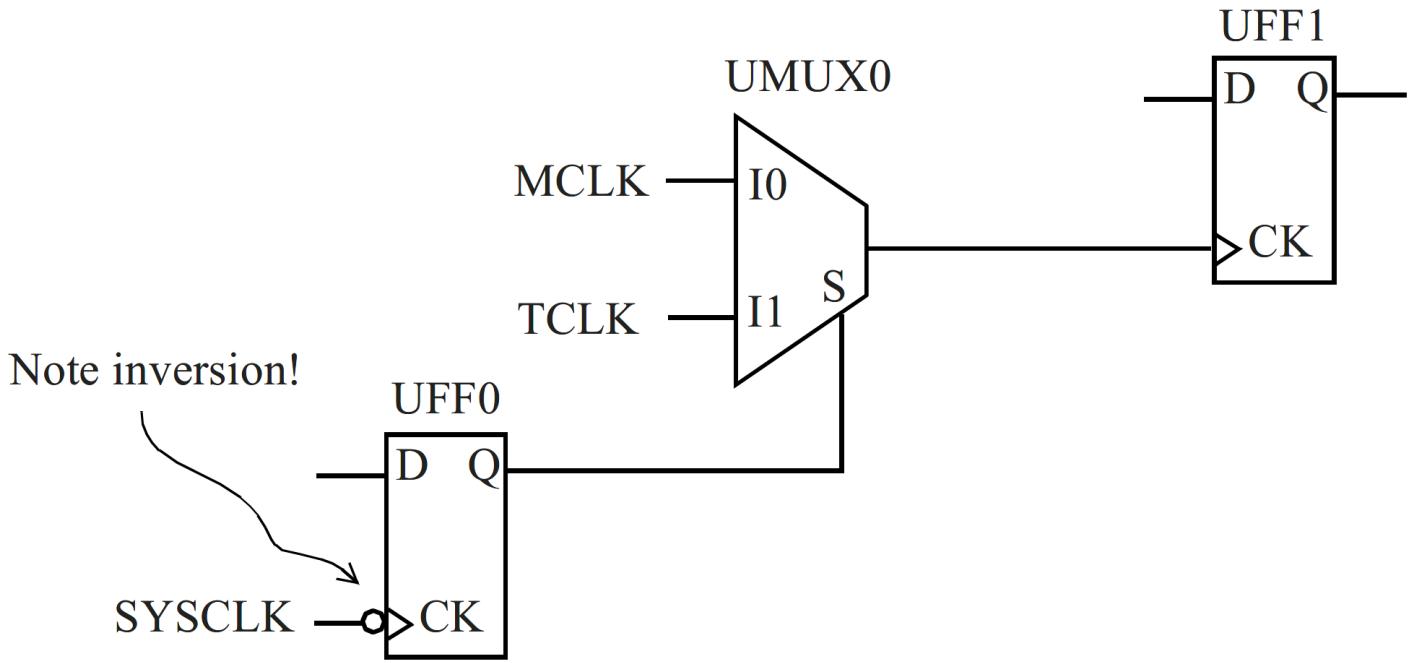


Figure 9 Clock gating using a multiplexer.

A clock gating check at the multiplexer inputs ensures that the multiplexer select signal arrives at the right time to cleanly switch between MCLK and TCLK.

Clock Gating Checks---Clock Gating with a Multiplexer

Figure 10 shows the timing relationships. The select signal for the multiplexer must arrive at the time MCLK is low. Also, assume TCLK will be low when select changes.

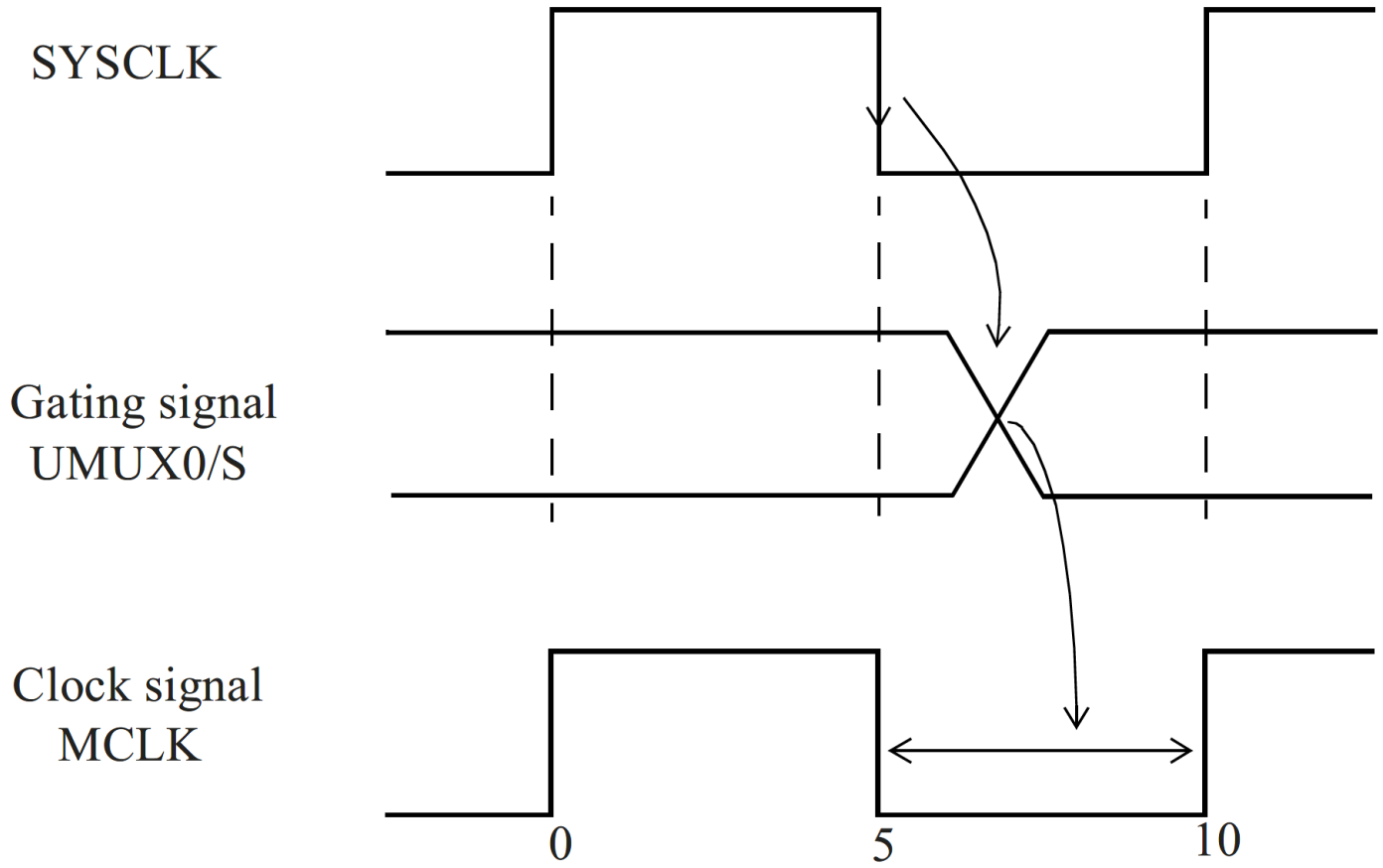


Figure 10 Gating signal arrives when clock is low.

Clock Gating Checks---Clock Gating with a Multiplexer

Since the gating cell is a multiplexer, the clock gating check is not inferred automatically, as evidenced in this message reported during STA.

Warning: No clock-gating check is inferred for clock MCLK at pins UMUX0/S and UMUX0/I0 of cell UMUX0.

Warning: No clock-gating check is inferred for clock TCLK at pins UMUX0/S and UMUX0/I1 of cell UMUX0.

Clock Gating Checks---Clock Gating with a Multiplexer

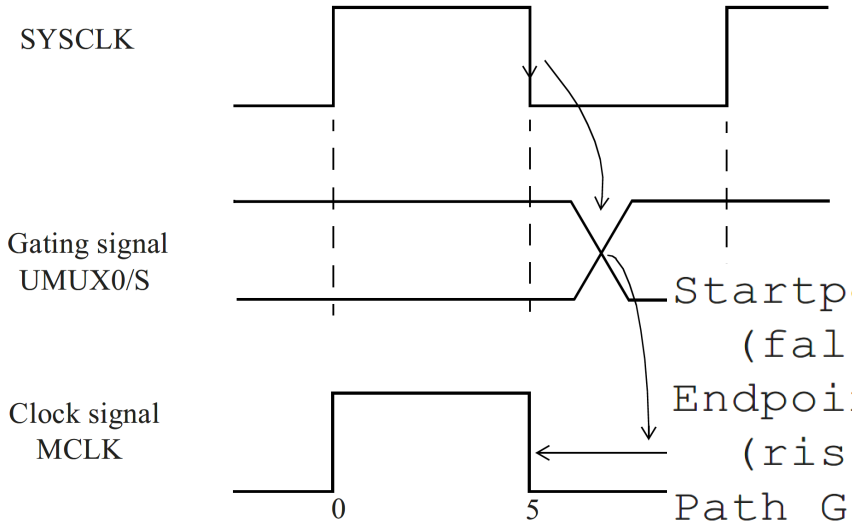
However a clock gating check can be explicitly forced by providing a set_clock_gating_check specification.

- *set_clock_gating_check -high [get_cells UMUX0]*
- *set_disable_clock_gating_check UMUX0/I1*

- The disable check turns off the clock gating check on the specific pin, as we are not concerned with this pin.
- The clock gating check on the multiplexer has been specified to be an active-high clock gating check.

Clock Gating Checks---Clock Gating with a Multiplexer

Here is the setup timing path report.




```
Startpoint: UFF0
  (falling edge-triggered flip-flop clocked by SYSCLK)
Endpoint: UMUX0
  (rising clock gating-check end-point clocked by MCLK)
Path Group: **clock_gating_default**
Path Type: max
```

Point	Incr	Path
clock SYSCLK (fall edge)	**5.00**	5.00
clock source latency	0.00	5.00
SYSCLK (in)	0.00	5.00 f
UFF0/CKN (DFN)	0.00	5.00 f
UFF0/Q (DFN)	0.15	5.15 r
UMUX0/S (MUX2)	0.00	5.15 r
data arrival time		5.15

Clock Gating Checks---Clock Gating with a Multiplexer

```
clock MCLK (rise edge)                    10.00      10.00
clock source latency                       0.00      10.00
MCLK (in)                                  0.00      10.00 r
UMUX0/I0 (MUX2  )                          0.00      10.00 r
clock gating setup time                    0.00      10.00
data required time                                   10.00
-----------------------------------------------------------
data required time                                   10.00
data arrival time                                    -5.15
-----------------------------------------------------------
slack (MET)                                           4.85
```

Clock Gating Checks---Clock Gating with a Multiplexer

Here is the clock gating hold timing report.

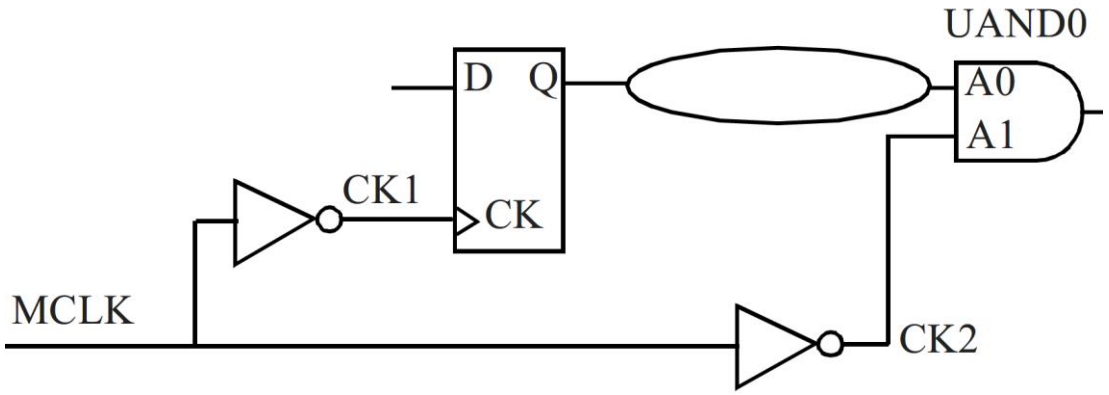
```
Startpoint: UFF0
  (falling edge-triggered flip-flop clocked by SYSCLK)
Endpoint: UMUX0
  (rising clock gating-check end-point clocked by MCLK)
Path Group: **clock_gating_default**
Path Type: min

Point                                          Incr       Path
-----------------------------------------------------------------
clock SYSCLK (fall edge)                       5.00       5.00
clock source latency                           0.00       5.00
SYSCLK (in)                                    0.00       5.00 f
UFF0/CKN (DFN  )                               0.00       5.00 f
UFF0/Q (DFN  )                                 0.13       5.13 f
UMUX0/S (MUX2  )                               0.00       5.13 f
data arrival time                                         5.13
```

Clock Gating Checks---Clock Gating with a Multiplexer

```
clock MCLK (fall edge)                  5.00        5.00
clock source latency                    0.00        5.00
MCLK (in)                               0.00        5.00 f
UMUX0/I0 (MUX2  )                       0.00        5.00 f
clock gating hold time                  0.00        5.00
data required time                                  5.00
-------------------------------------------------------
data required time                                  5.00
data arrival time                                  -5.13
-------------------------------------------------------
slack (MET)                                         0.13
```

Clock Gating Checks---Clock Gating with Clock Inversion

Figure 11 shows another clock gating example where the clock to the flip-flop is inverted and the output of the flip-flop is the gating signal.



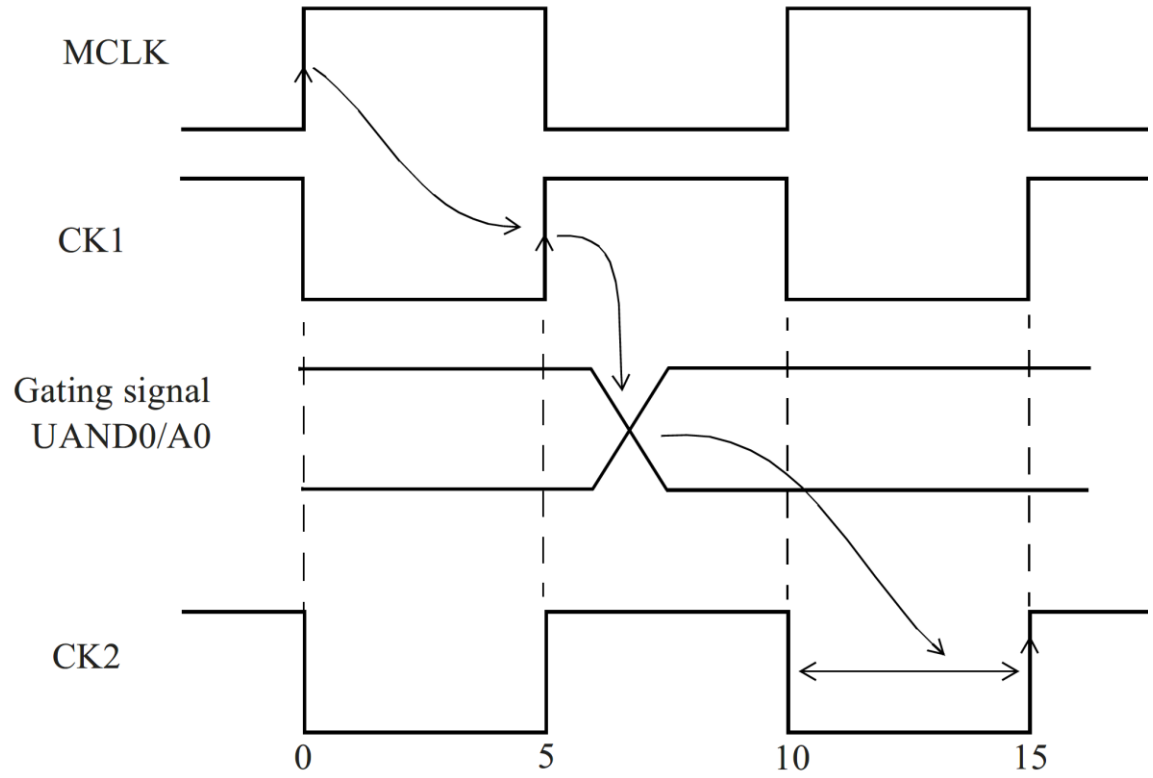


Figure 11 Clock gating example with clock inversion.

Since the gating cell is an *and* cell, the gating signal must switch only when the clock signal at the and cell is low. This defines the setup and hold clock gating checks.

Clock Gating Checks---Clock Gating with Clock Inversion

Here is the clock gating setup timing report.

```
Startpoint: UDFF0
  (rising edge-triggered flip-flop clocked by MCLK')
Endpoint: UAND0
  (rising clock gating-check end-point clocked by MCLK')
Path Group: **clock_gating_default**
Path Type: max

Point                                          Incr       Path
-----------------------------------------------------------------
clock MCLK' (rise edge)                        5.00       5.00
clock source latency                           0.00       5.00
MCLK (in)                                      0.00       5.00 f
UINV0/ZN (INV  )                               0.02       5.02 r
UDFF0/CK (DF  )                                0.00       5.02 r
UDFF0/Q (DF  )                                 0.13       5.15 f
UAND0/A1 (AN2  )                               0.00       5.15 f
data arrival time                                         5.15
```

Clock Gating Checks---Clock Gating with Clock Inversion

```
clock MCLK' (rise edge)                  15.00       15.00
clock source latency                      0.00       15.00
MCLK (in)                                 0.00       15.00 f
UINV1/ZN (INV  )                          0.02       15.02 r
UAND0/A2 (AN2  )                          0.00       15.02 r
clock gating setup time                   0.00       15.02
data required time                                   15.02
-----------------------------------------------------------
data required time                                   15.02
data arrival time                                    -5.15
-----------------------------------------------------------
slack (MET)                                           9.87
```

Clock Gating Checks---Clock Gating with Clock Inversion

Here is the clock gating hold timing report.

```
Startpoint: UDFF0
  (rising edge-triggered flip-flop clocked by MCLK')
Endpoint: UAND0
  (rising clock gating-check end-point clocked by MCLK')
Path Group: **clock_gating_default**
Path Type: min

Point                                          Incr       Path
-----------------------------------------------------------------
clock MCLK' (rise edge)                        5.00       5.00
clock source latency                           0.00       5.00
MCLK (in)                                      0.00       5.00 f
UINV0/ZN (INV  )                               0.02       5.02 r
UDFF0/CK (DF  )                                0.00       5.02 r
UDFF0/Q (DF  )                                 0.13       5.15 r
UAND0/A1 (AN2  )                               0.00       5.15 r
data arrival time                                         5.15
```

Clock Gating Checks---Clock Gating with Clock Inversion

```
clock MCLK' (fall edge)                  10.00       10.00
clock source latency                      0.00       10.00
MCLK (in)                                 0.00       10.00 r
UINV1/ZN (INV  )                          0.01       10.01 f
UAND0/A2 (AN2  )                          0.00       10.01 f
clock gating hold time                    0.00       10.01
data required time                                   10.01
-------------------------------------------------------------
data required time                                   10.01
data arrival time                                    -5.15
-------------------------------------------------------------
slack (VIOLATED)                                     -4.86
```

The hold check validates whether the data (gating signal) changes before the falling edge of MCLK at time 10ns.

Clock Gating Checks---Clock Gating with Clock Inversion

In the event that the gating cell is a complex cell and the setup and hold checks are not obvious, the set_clock_gating_check command can be used to specify a setup and hold check on the gating signal that gates a clock signal.

- *set_clock_gating_check -setup 2.4 -hold 0.8 [get_cells U0/UXOR1]*

 # Specifies the setup and hold time for the clock

 # gating check at the specified cell.

- *set_clock_gating_check -high [get_cells UMUX5]*

 # Check is performed on high level of clock. Alternately, the -low option can be used for an active-low clock gating check.

参考书目

- Static Timing Analysis for Nanometer Designs: A Practical Approach. J. Bhasker, Rakesh Chadha. Springer Science Business Media, LLC 2009. Chaper 10.

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