数字集成电路静态时序分析基础

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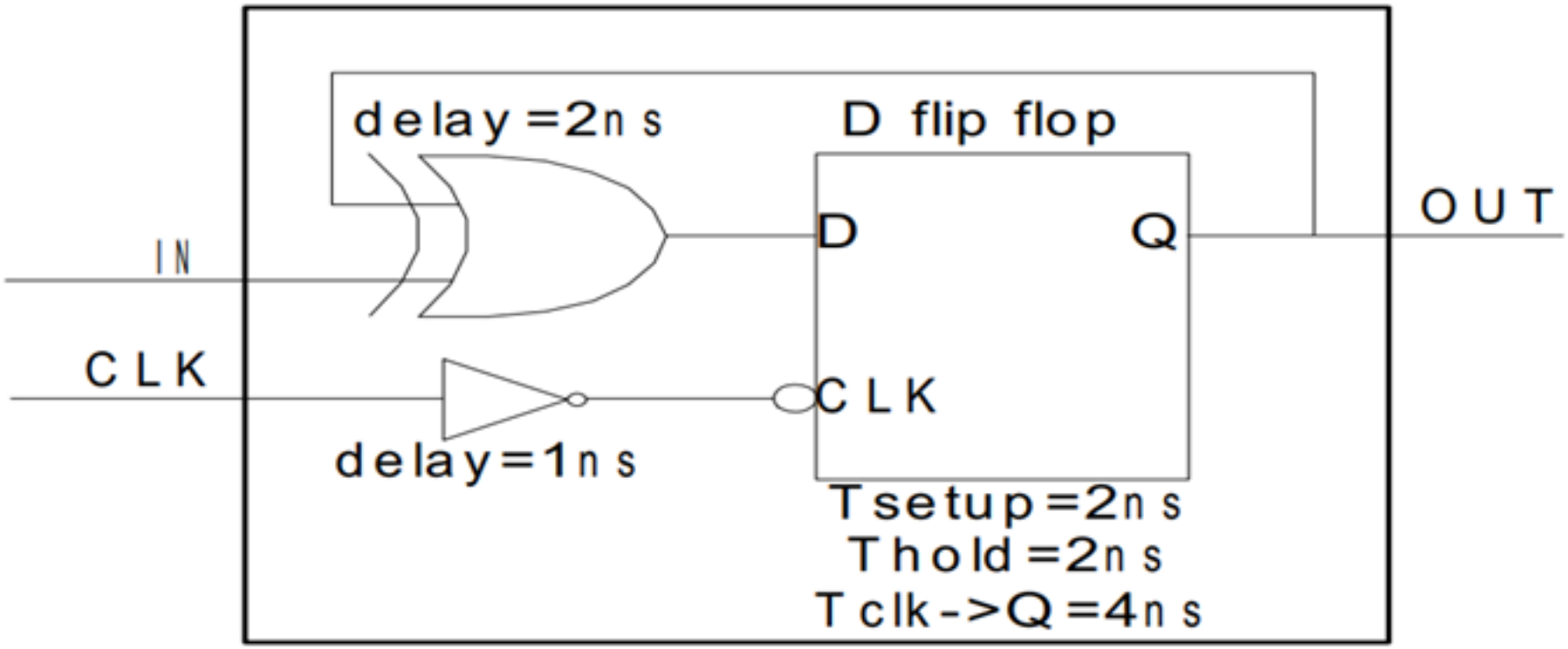
习题-1



如果把上述电路整体看为一个触发器，请回答如下问题

习题-1

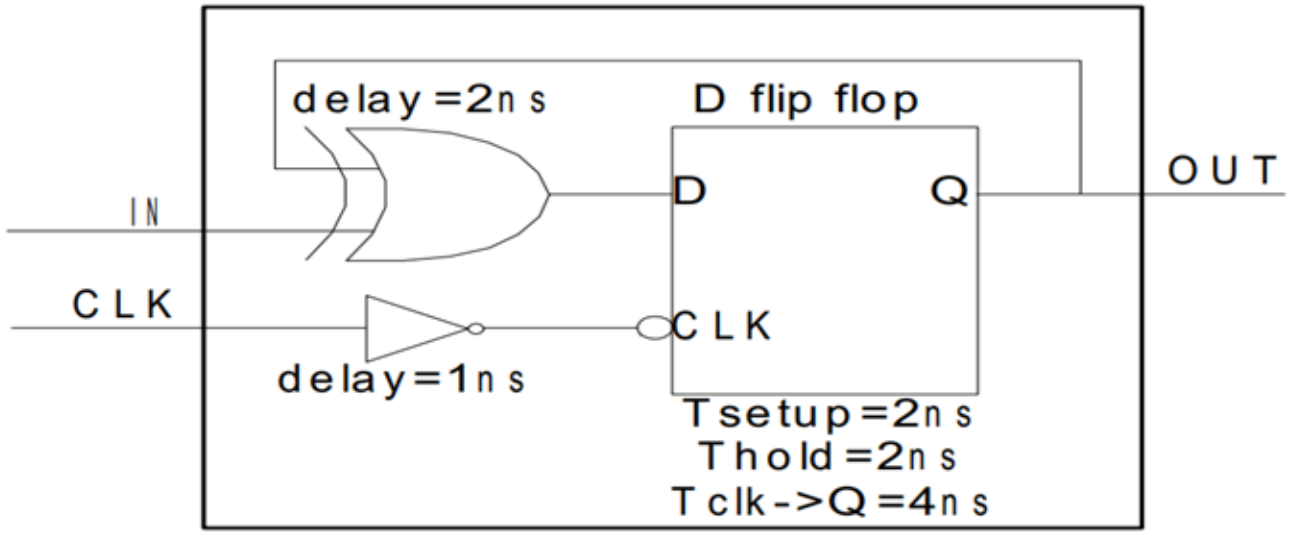
(1)[8分]该电路的有效建立时间和保持时间是多少?

A. Tsetup = 4 ns, Thold = 1 ns

B. Tsetup = 3 ns, Thold = 0 ns

C. Tsetup = 3 ns, Thold = 1ns

D. Tsetup = 2 ns, Thold = 0 ns



习题-1

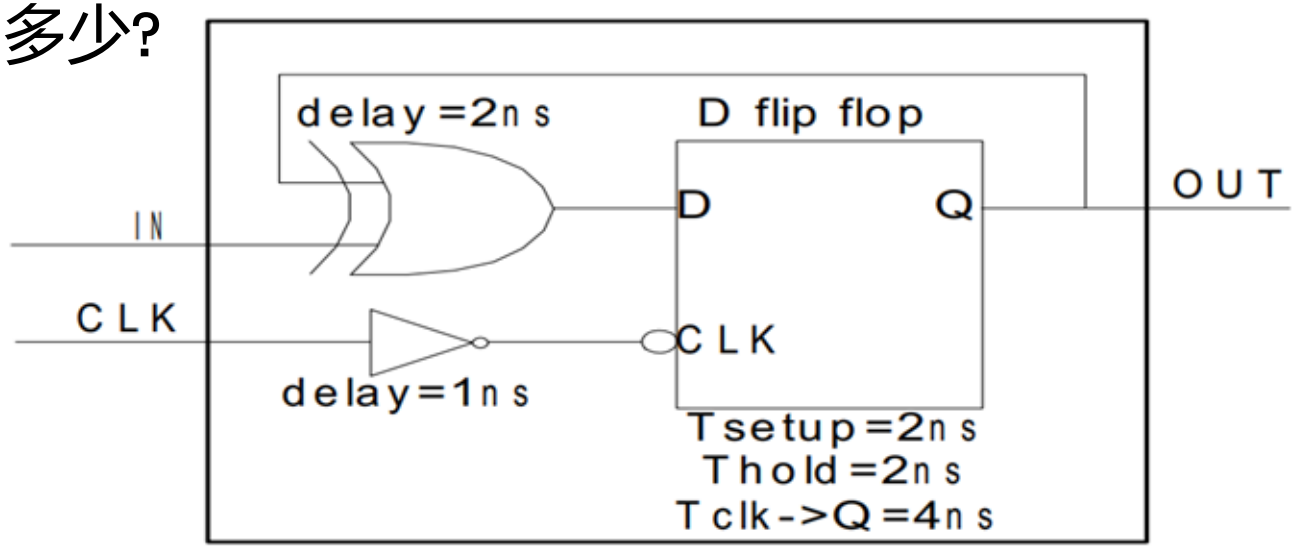
(2) [8分]该电路的最高时钟频率为多少?

A. 250 MHz

B. 80 MHz

C. 125 MHz

D. 166.7 MHz



习题-1

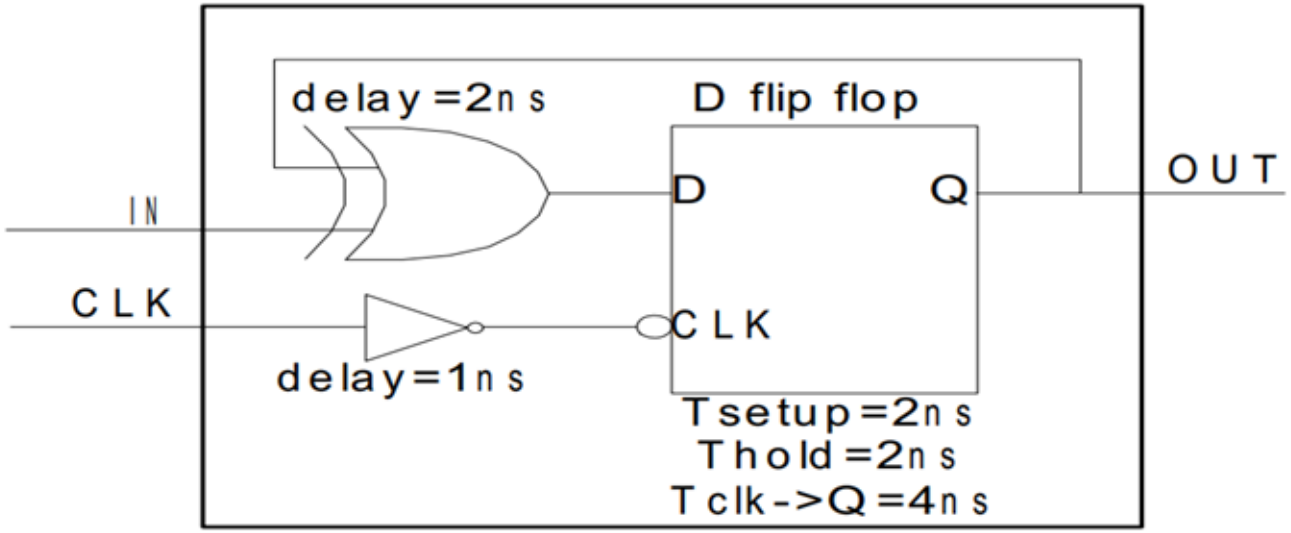
(3) [5分]该电路的功能与下列哪个触发器相似?

A. D flip flop with enable

B. T flip flop

C. JK flip flop

D. SR flip flop



习题-1

(4) [4分]对于一个同步电路，以下哪个公式可以用于计算最高工作频率?

A. Max Freq = 1/(Tprop_delay + Tsu + Thold)

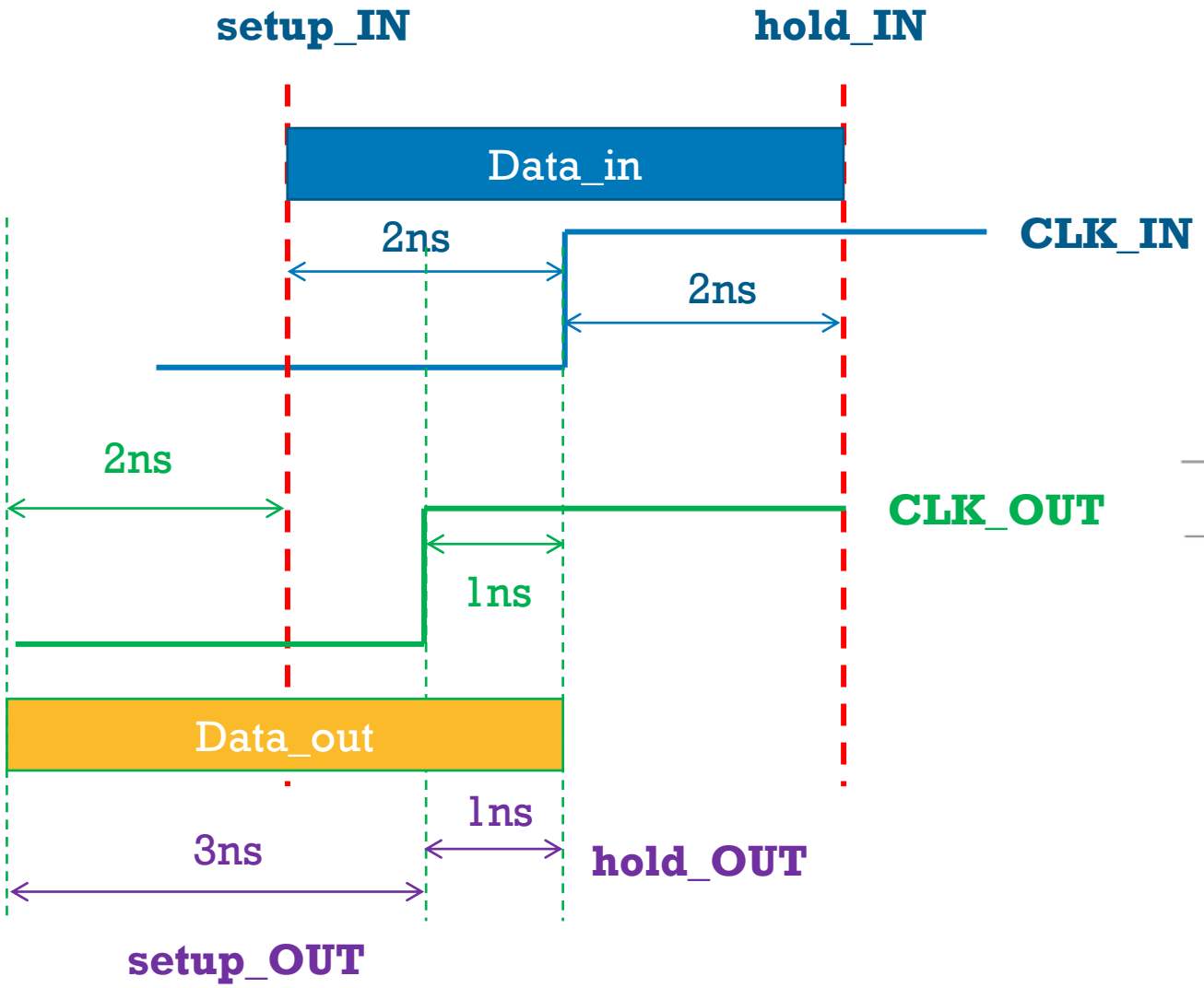
B. Max Freq = 1/(Tprop_delay + Tsu + Tco + Thold)

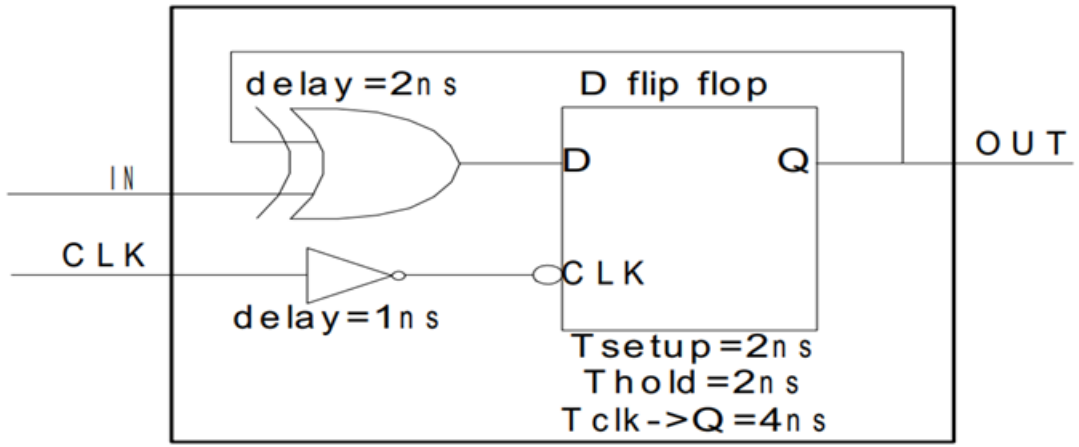
C. Max Freq = 1/(Tsu + Tco + Thold + Tclock_skew)

D. Max Freq = 1/(Tprop_delay + Tsu + Tco + Tclock_skew)

E. Max Freq = 1/(Tprop_delay + Tsu + Thold + Tco + Tclock_skew)

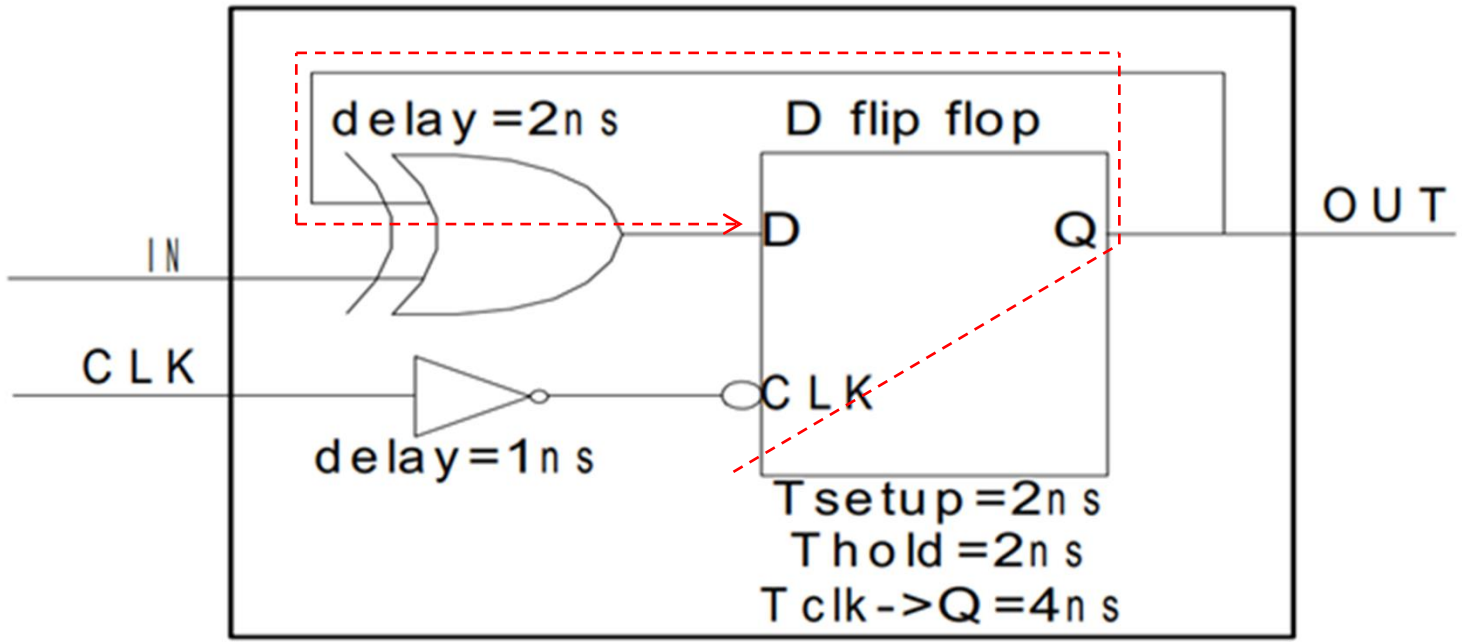
习题-1





(1) C. Tsetup = 3 ns, Thold = 1ns

习题-1



(2) [8分]该电路的最高时钟频率为多少?

C. 125 MHz

习题-1

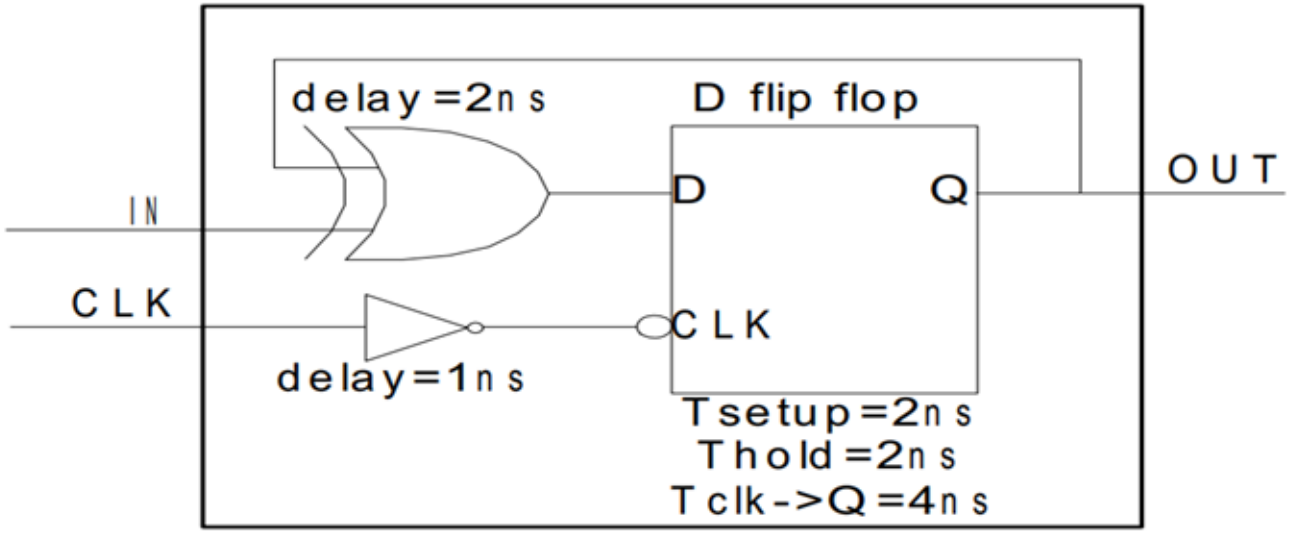
(3) [5分]该电路的功能与下列哪个触发器相似?

A. D flip flop with enable

B. T flip flop

C. JK flip flop

D. SR flip flop



习题-1

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C. Max Freq = 1/(Tsu + Tco + Thold + Tclock_skew)

D. Max Freq = 1/(Tprop_delay + Tsu + Tco + Tclock_skew)

E. Max Freq = 1/(Tprop_delay + Tsu + Thold + Tco + Tclock_skew)

习题-2

Please reference the following for the next group of questions

Startpoint: fifo_rd_pd_reg_16_
(rising edge-triggered flip-flop clocked by my_clock)

Endpoint: we_bank_0_reg_2_
(rising edge-triggered flip-flop clocked by my_clock)

Path Group: my_group

Path Type: max

Point	Cap	Trans	Incr	Path
clock my_clock (rise edge)			0.0000	0.0000
clock network delay (ideal)			0.0000	0.0000
fifo_rd_pd_reg_16_/CK (p_SDFFHX4)			0.0000	0.0000 0.0000 r
fifo_rd_pd_reg_16_/Q (p_SDFFHX4)	0.0226	0.0542	0.1166	0.1166 f
obuf_U1904/Y (NAND3BX4)	0.0095	0.0643	0.0915	0.2082 f

习题-2

obuf_U1903/Y (INVX8)	0.0188	0.0450	0.0385	0.2467 r
obuf_buf_1_add_524_U14/Y (NAND2X4)	0.0088	0.0431	0.0374	0.2841 f
U7015/Y (OAI21X4)	0.0111	0.1008	0.0781	0.3622 r
U22745/Y (AOI21X4)	0.0054	0.0481	0.0294	0.3916 f
obuf_U9743/Y (OAI21X4)	0.0067	0.0772	0.0638	0.4554 r
obuf_buf_1_add_524_U57/Y (XNOR2X4)	0.0098	0.1071	0.0769	0.5323 r
DP_OP_248_5346_8_U51/CO0 (AFCSHCINX2)	0.0037	0.0970	0.1378	0.6702 r
obuf_U9662/Y (MX2X4)	0.0077	0.0382	0.0825	0.7527 r
DP_OP_248_5346_8_U44/S (AFCSHCINX4)	0.0075	0.0462	0.1200	0.8726 f
obuf_U9746/Y (INVX6)	0.0174	0.0463	0.0394	0.9120 r
obuf_U1772/Y (NOR2X4)	0.0113	0.0554	0.0294	0.9414 f
U17999/Y (OA22X4)	0.0058	0.0398	0.1128	1.0542 f
obuf_U1852/Y (NOR2X4)	0.0116	0.0909	0.0686	1.1228 r
U26782/Y (INVX10)	0.0549	0.0558	0.0538	1.1765 f
U7011/Y (OA22X4)	0.0092	0.0465	0.0982	1.2747 f

习题-2

U27252/Y (CLKNAND2X2)	0.0057	0.0484	0.0402	1.3149 r
U24494/Y (XOR2X3)	0.0058	0.0531	0.0386	1.3536 f
obuf_U3105/Y (NOR2X4)	0.0056	0.0583	0.0497	1.4033 r
obuf_U3097/Y (NAND2X4)	0.0056	0.0341	0.0329	1.4362 f
obuf_U3094/Y (NOR2X4)	0.0053	0.0534	0.0421	1.4784 r
obuf_U1886/Y (AOI21X4)	0.0157	0.0607	0.0580	1.5364 f
obuf_U1861/Y (NOR3X4)	0.0101	0.1561	0.1036	1.6400 r
U24496/Y (INVX4)	0.0073	0.0442	0.0351	1.6751 f
obuf_U1760/Y (OR2X4)	0.0135	0.0378	0.0731	1.7481 f
obuf_U9462/Y (INVX12)	0.0325	0.0428	0.0358	1.7839 r
U17857/Y (OAI211X4)	0.0062	0.0992	0.0506	1.8345 f
U24495/Y (CLKINVX6)	0.0036	0.0334	0.0188	1.8533 r
we_bank_0_reg_2_/D (p_SDFFRHQX4)		0.0334	0.0000	1.8533 r
data arrival time			1.8533	

习题-2

clock my_clock (rise edge)	1.8000	1.8000
clock network delay (ideal)	0.0000	1.8000
we_bank_0_reg_2_/CK (p_SDFFRHQX4)	0.0000	1.8000 r
library setup time	-0.0701	1.7299
data required time		1.7299
---		
data required time		1.7299
data arrival time		-1.8533
---		
slack (VIOLATED)		-0.1234

习题-2

What does the above information represent?

What type of tool might have produced the above report?

What is the name and frequency of the clock referenced?

What frequency can the circuit above actually run at?

How many levels of logic are there between the two flip-flops

What component has the greatest delay through it?

What is the setup time of the last flip flop in the path

What is the hold time of the last flip flop in the path

What assumptions can you make about operating conditions from this report?

Would this report be useful near the end (tape-out) of a chip?

习题-2

What does the above information represent?

A: It is PT/DC timing report. It shows there is a –0.1234ns reg2reg setup violation.

习题-2

5. What type of tool might have produced the above report?

A: The report comes from Synopsys PT and DC. Encounter and other tools with STA function can create the similar report, but with different format.

习题-2

6. What is the name and frequency of the clock referenced?

A: Clock name is "my_clock" and frequency is 1/1.8ns

习题-2

7. What frequency can the circuit above actually run at?

A: 1/1.9234ns

注意：不是 1/1.8533ns 哟，setup 时间也要加上

clock my_clock (rise edge)	1.8000	1.8000
clock network delay (ideal)	0.0000	1.8000
we_bank_0_reg_2_/CK (p_SDFFRHQX4)	0.0000	1.8000 r
library setup time	-0.0701	1.7299
data required time		1.7299
---		
data required time		1.7299
data arrival time		-1.8533
---		
slack (VIOLATED)		-0.1234

$$T_{launch} + T_{ck2q} + T_{dp} < T_{capture} + T_{cycle} - T_{setup}$$

习题-2

8. How many levels of logic are there between the two flip-flops

A: 28

习题-2

9. What component has the greatest delay through it?

A: P_OP_248_5346_8_U51(AFCSHCINX2)

(except the flops)

习题-2

10. What is the setup time of the last flip flop in the path

A: 0.0701ns

clock my_clock (rise edge)	1.8000	1.8000
clock network delay (ideal)	0.0000	1.8000
we_bank_0_reg_2_/CK (p_SDFFRHQX4)	0.0000	1.8000 r
library setup time	-0.0701	1.7299
data required time		1.7299
---		
data required time		1.7299
data arrival time		-1.8533
---		
slack (VIOLATED)		-0.1234

习题-2

11. What is the hold time of the last flip flop in the path

A: There is no information about hold time in this report.

习题-2

12. What assumptions can you make about operating conditions from this report?

A: Worst Case

习题-2

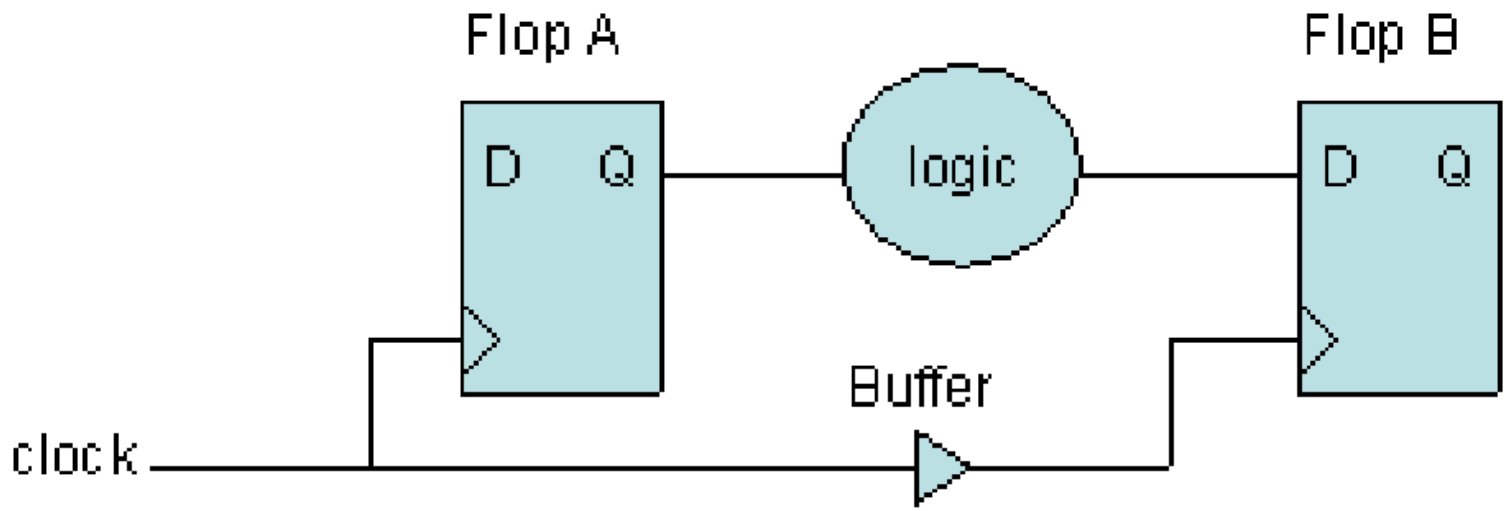
13. Would this report be useful near the end (tape-out) of a chip? Please explain your answer.

A: No. The main reason is clock insertion delay was not in the report.

--> clock network delay (ideal)

Point	Cap	Trans	Incr	Path	
clock my_clock (rise edge)			0.0000	0.0000	
clock network delay (ideal)			0.0000	0.0000	
fifo_rd_pd_reg_16_/CK (p_SDFFHX4)			0.0000	0.0000	0.0000 r
fifo_rd_pd_reg_16_/Q (p_SDFFHX4)		0.0226	0.0542	0.1166	0.1166 f
obuf_U1904/Y (NAND3BX4)		0.0095	0.0643	0.0915	0.2082 f

习题-3



What parameters do you need to know to calculate the timing of the above circuit?

15. Using the parameters from #14, write the equation that needs to be fulfilled in order for the above circuit to meet setup time on Flop B. Assume parameters are max delay.

16. Using the parameters from #14, write the equation that needs to be fulfilled in order for the above circuit to meet hold time on Flop B. Assume parameters are min delay.

习题-3

14. What parameters do you need to know to calculate the timing of the above circuit?

A: All following max and min delay information is requested.

Flop A: ck->Q

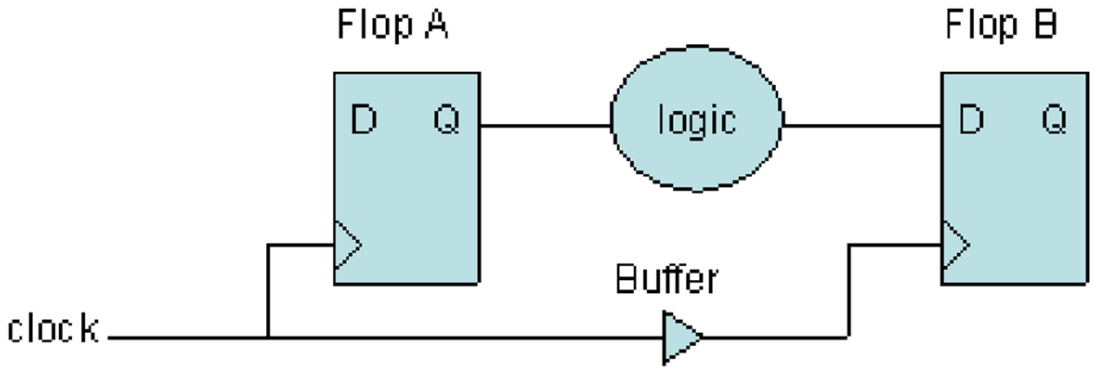
Logic : input -> output

Buffer : input -> output

And

flop B: setup and hold timing requirement.

Clock: period and uncertainty



$$T_{launch} + T_{ck2q} + T_{dp} < T_{capture} + T_{cycle} - T_{setup}$$

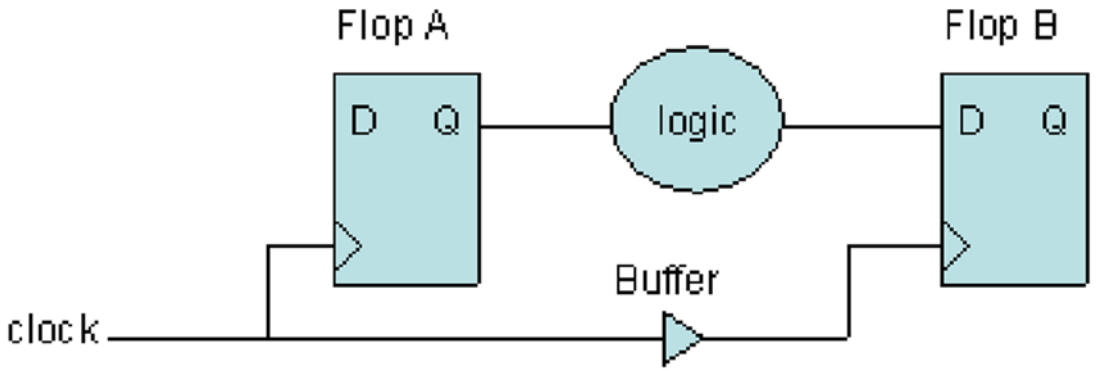
习题-3

15. Using the parameters from #14, write the equation that needs to be fulfilled in order for the above circuit to meet setup time on Flop B. Assume parameters are max delay.

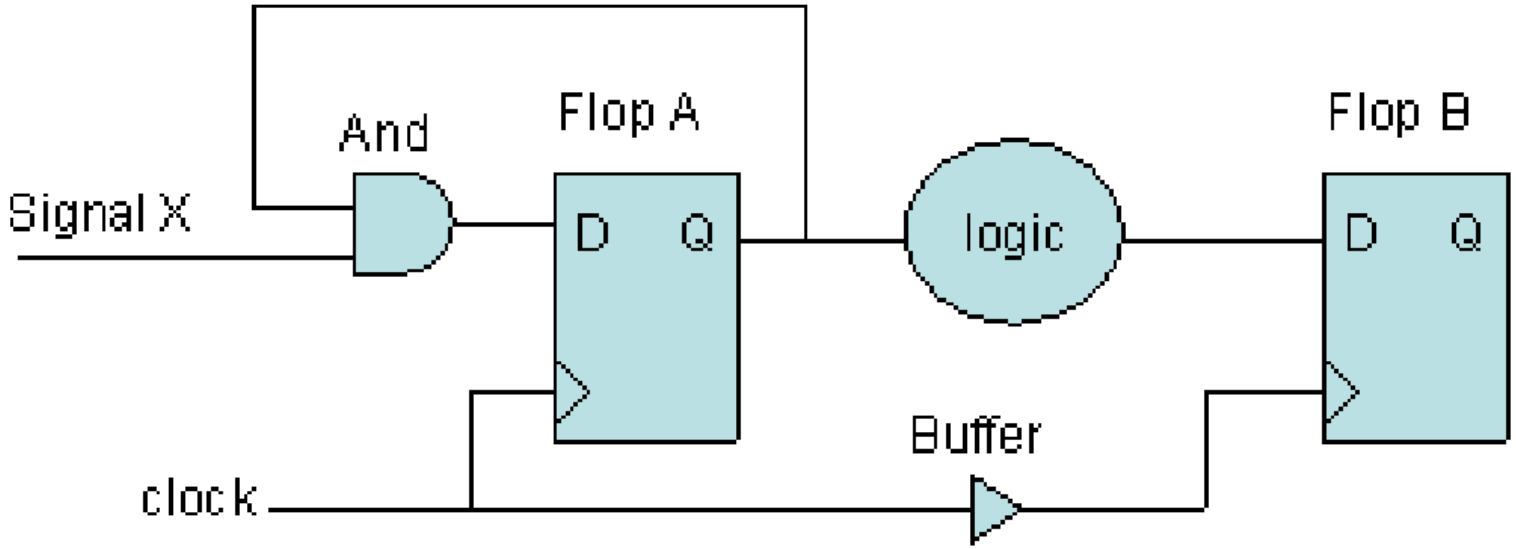
A: clock(period) + Buffer(delay) – flopB(setup) - clock(uncertainty) >= flopA(ck->Q) + logic(delay)

16. Using the parameters from #14, write the equation that needs to be fulfilled in order for the above circuit to meet hold time on Flop B. Assume parameters are min delay.

A: FlopB(hold) + Buffer(delay) <= flopA(ck->Q) + logic(delay)



习题-3



17. What new parameters do you need to know to calculate the timing of the above circuit?

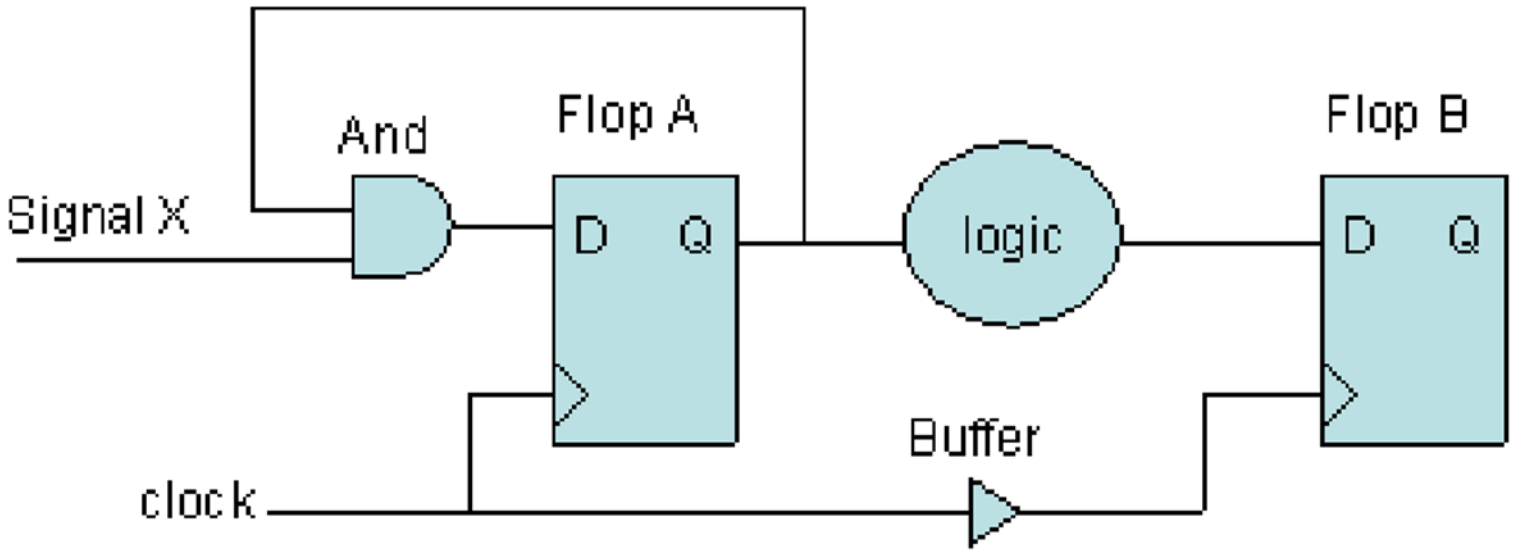
18. Are there new issues that are of concern with the addition of the new gate and input signal? Please describe in detail

习题-3

17. What new parameters do you need to know to calculate the timing of the above circuit?

A: And: max and min delay

SignalX: max and min input delay

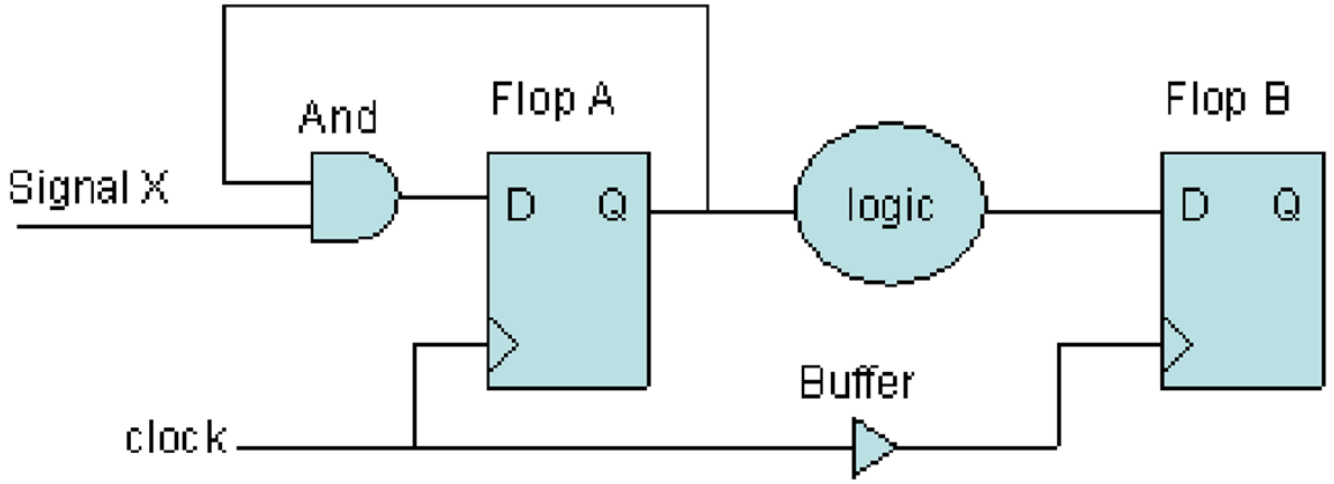


习题-3

18. Are there new issues that are of concern with the addition of the new gate and input signal? Please describe in detail

A: need to check setup and hold timing for flopA using And gate and Signal X input delay. The setup and hold timing for FlopB should be verified again because the change of output loading at FlopA Q pin.

Flop A负载的增加会引起A到B之间路径延迟的变化，一般会被初学者忽略



谢谢聆听！

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