数字集成电路静态时序分析基础

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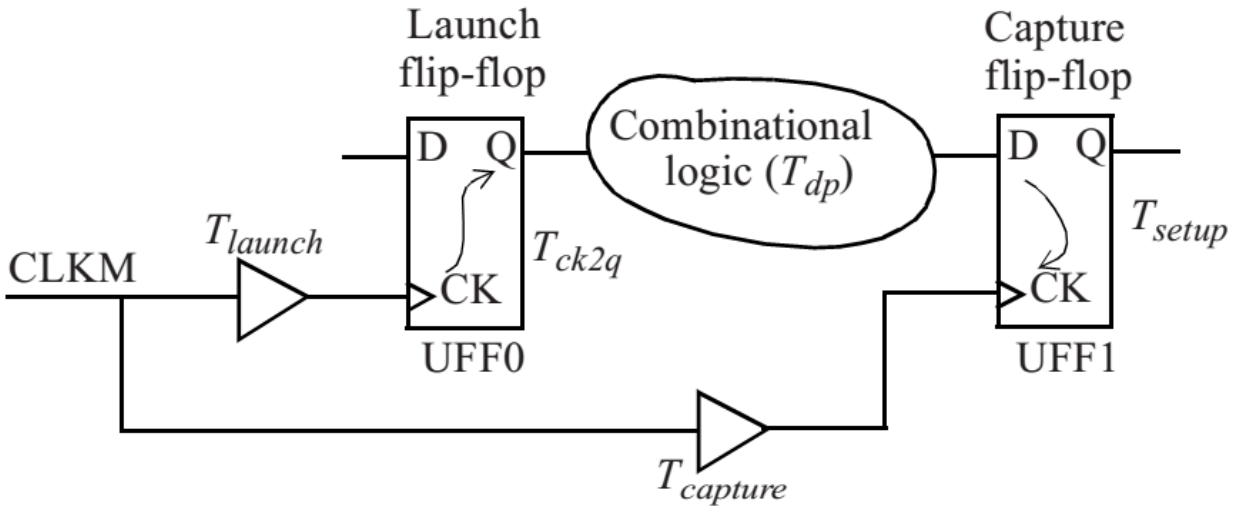
CONTENT

Part 5: Timing Verification

1. Setup timing check
2. Hold timing check

Setup Timing Check



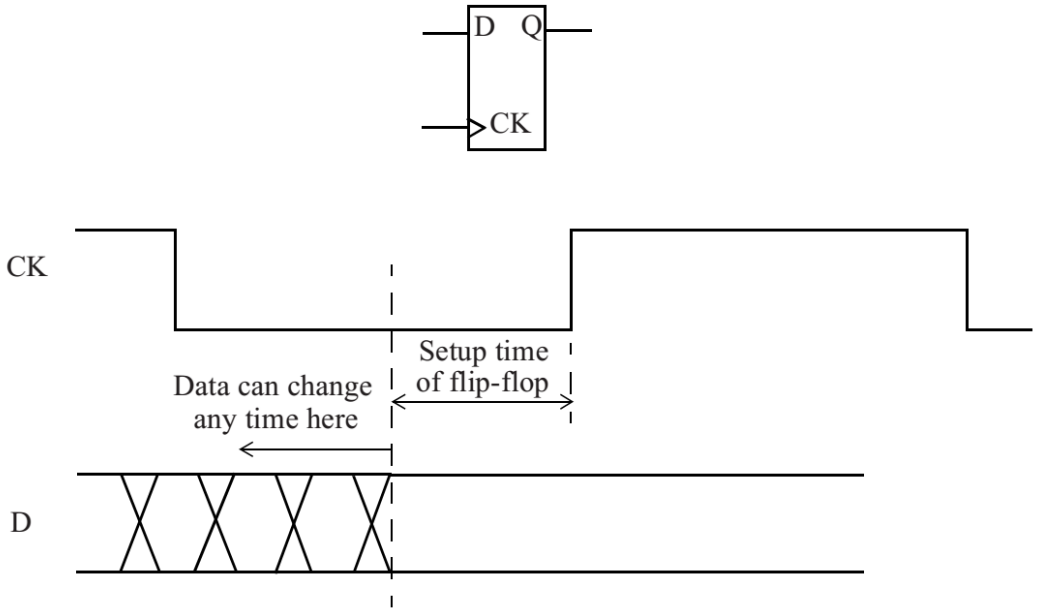
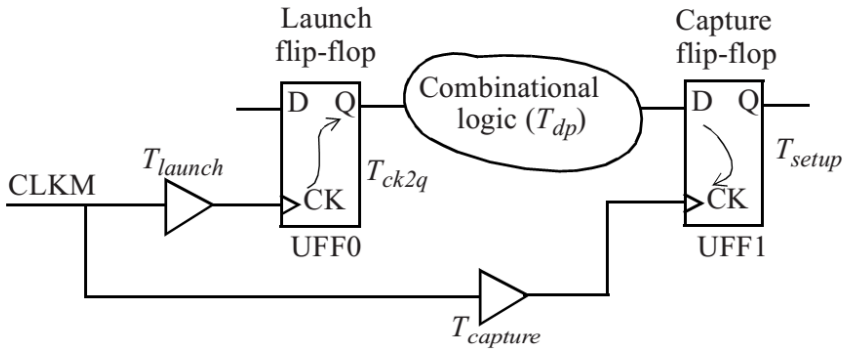
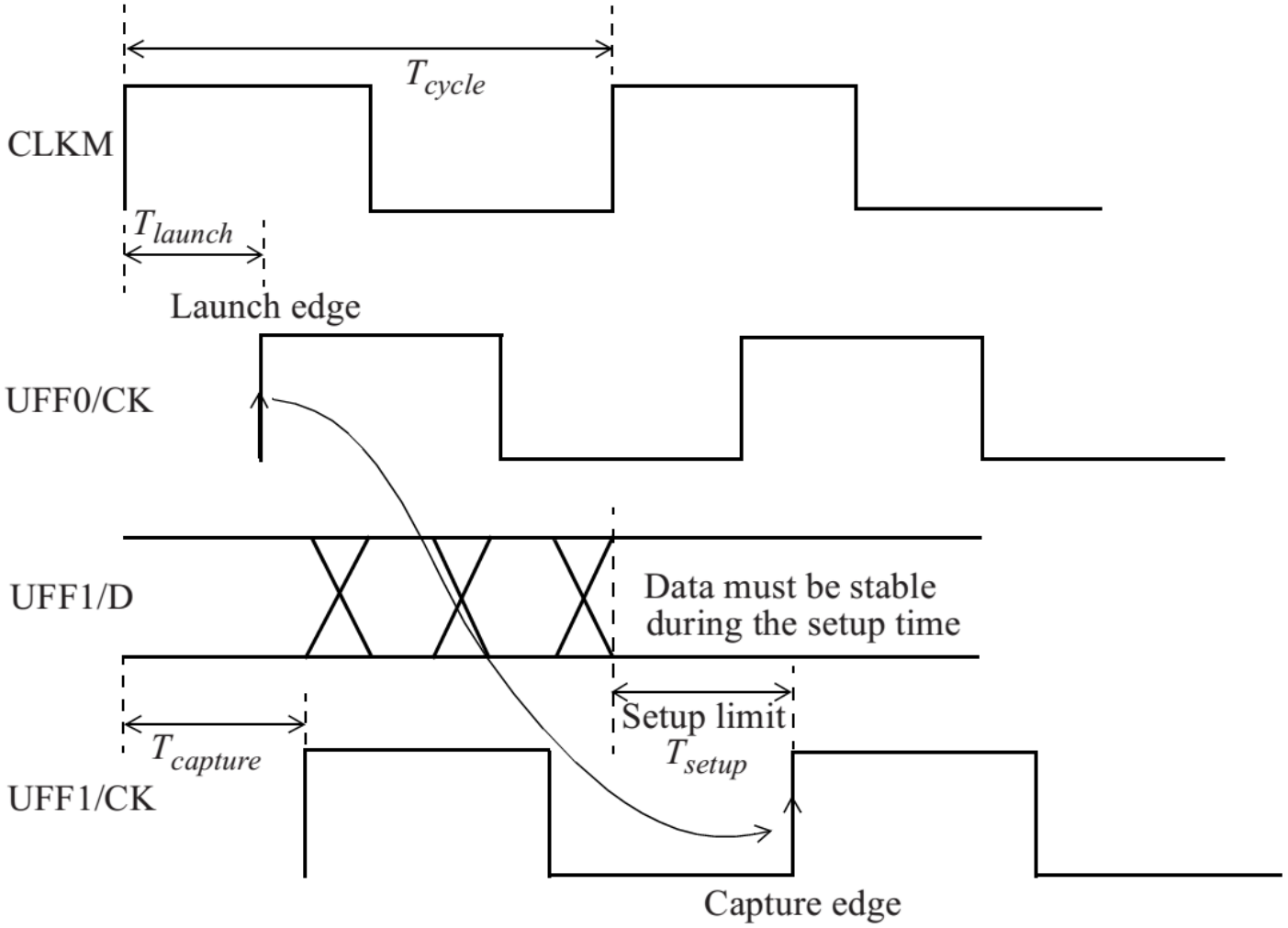


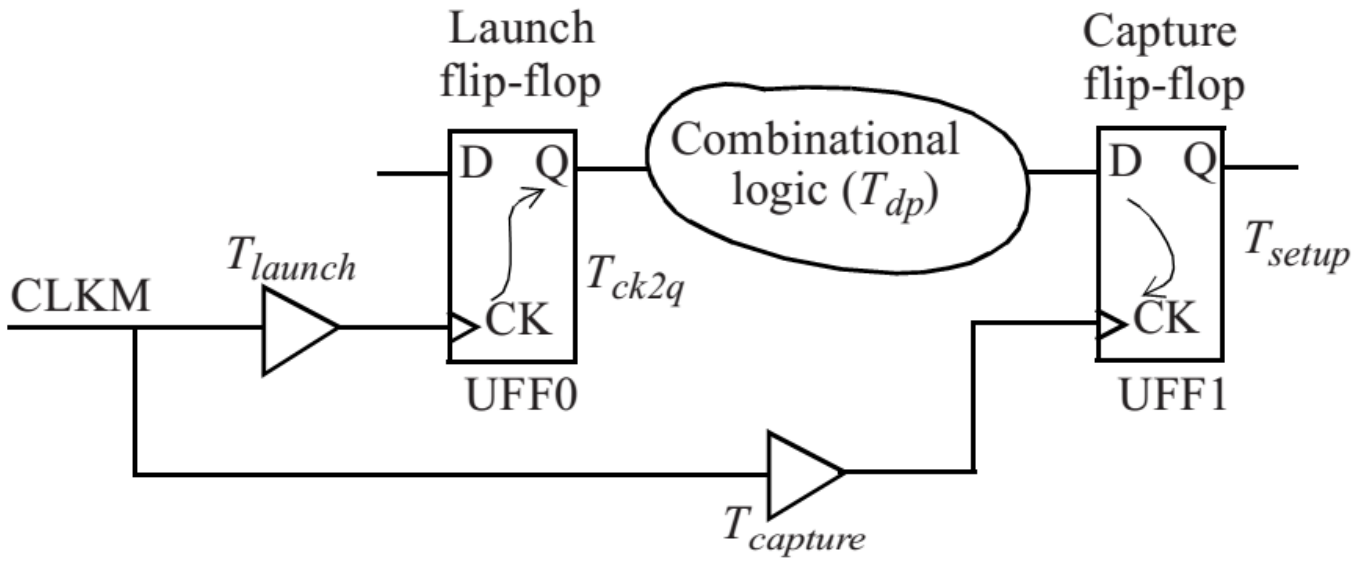
Figure 8-1 *Setup requirement of a flip-flop.*

Setup Timing Check





Setup Timing Check



The setup check can be mathematically expressed as:

$$T_{launch} + T_{ck2q} + T_{dp} < T_{capture} + T_{cycle} - T_{setup}$$

Setup Timing Check

1、Flip-flop to Flip-flop Path

Startpoint: UFF0 (**rising edge-triggered flip-flop clocked by CLKM**)
Endpoint: UFF1 (**rising edge-triggered flip-flop clocked by CLKM**)
Path Group: CLKM
Path Type: max

Point	Incr	Path
clock CLKM (rise edge)	**0.00**	0.00
clock network delay (ideal)	0.00	0.00
UFF0/CK (DFF)	0.00	0.00 r
UFF0/Q (DFF) <-	0.16	0.16 f
UNOR0/ZN (NR2)	0.04	0.20 r
UBUF4/Z (BUFF)	0.05	0.26 r
UFF1/D (DFF)	0.00	0.26 r
data arrival time		0.26

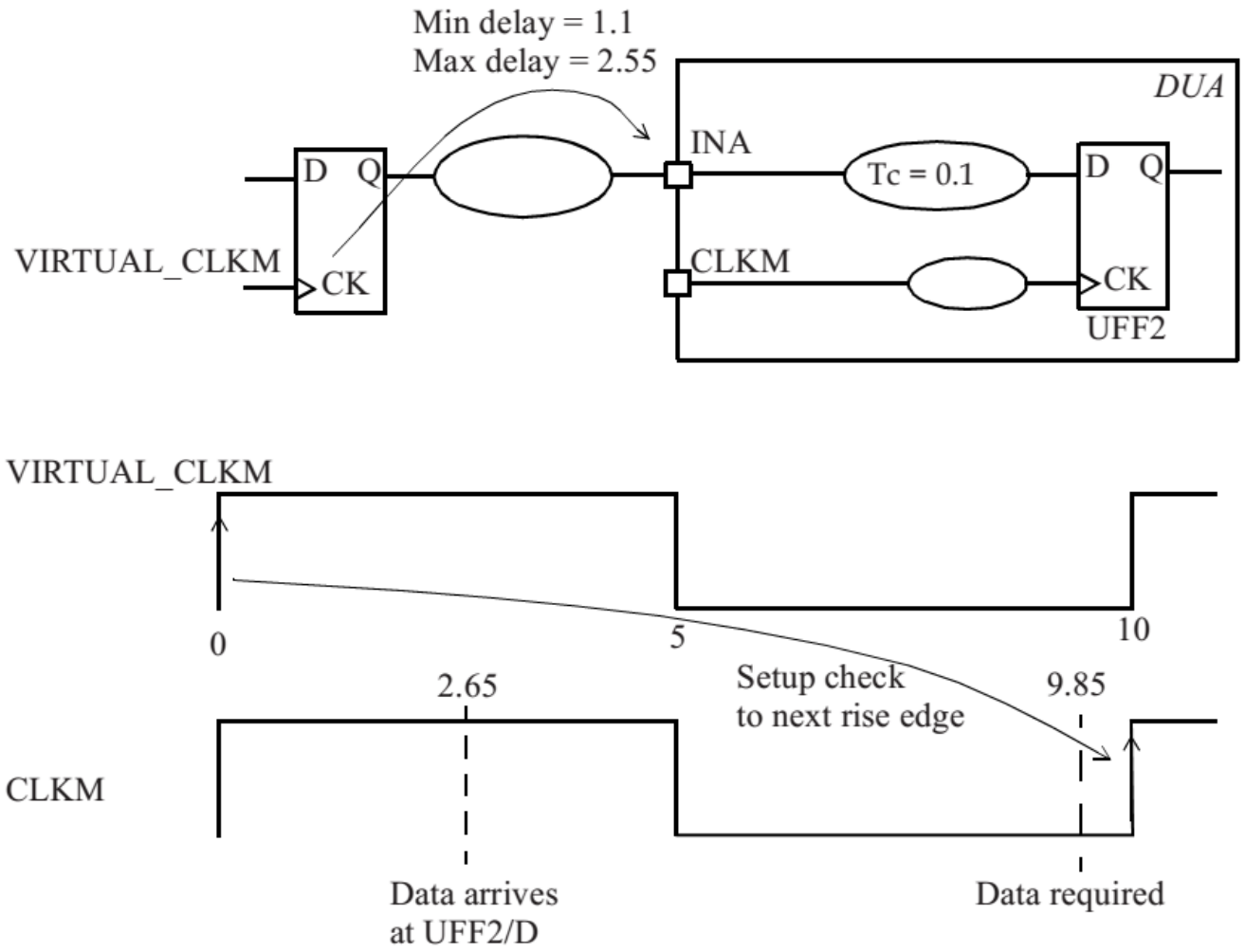
Setup Timing Check

1、Flip-flop to Flip-flop Path

```
clock CLKM (rise edge)                    10.00      10.00
clock network delay (ideal)                0.00      10.00
clock uncertainty                         -0.30       9.70
UFF1/CK (DFF )                                        9.70 r
library setup time                        -0.04       9.66
data required time                                    9.66
-------------------------------------------------------------
data required time                                    9.66
data arrival time                                    -0.26
-------------------------------------------------------------
slack (MET)                                           9.41
```

Setup Timing Check

2、Input to Flip-flop Path



Timing Analysis——Setup Timing Check

Constrain：

creat_clock –name VIRTUAL_CLKM –period 10 –waveform {0 5}

set_input_delay –clock VIRTUAL_CLKM –max 2.55 [get_ports INA]

Setup Timing Check

2、Input to Flip-flop Path

Startpoint: CIN (**input port clocked by CLKP**)
Endpoint: UFF4 (**rising edge-triggered flip-flop clocked by CLKP**)
Path Group: CLKP
Path Type: max

Point	Incr	Path
clock CLKP (rise edge)	0.00	0.00
clock network delay (propagated)	0.00	0.00
input external delay	**4.30**	4.30 f
CIN (in)	0.00	4.30 f
UBUF5/Z (BUFF)	0.06	4.36 f
UXOR1/Z (XOR2)	0.10	4.46 r
UFF4/D (DFF)	0.00	4.46 r
data arrival time		4.46
clock CLKP (rise edge)	12.00	12.00
clock source latency	0.00	12.00

Setup Timing Check

2、Input to Flip-flop Path

```
CLKP (in)                                    0.00      12.00 r
UCKBUF4/C (CKB  )                            0.06      12.06 r
UCKBUF5/C (CKB  )                            0.06      12.12 r
UFF4/CK (DFF )                               0.00      12.12 r
clock uncertainty                           -0.30      11.82
library setup time                          -0.05      11.77
data required time                                     11.77
-------------------------------------------------------------
data required time                                     11.77
data arrival time                                      -4.46
-------------------------------------------------------------
slack (MET)                                             7.31
```

3、Flip-flop to Output Path

Similar to the input port constraint described above, an output port can be constrained either with respect to a virtual clock, or an internal clock of the design, or an input clock port, or an output clock port.

To determine the delay of the last cell connected to the output port correctly, **one needs to specify the load on this port**. The output load is specified above using the **set_load** command.

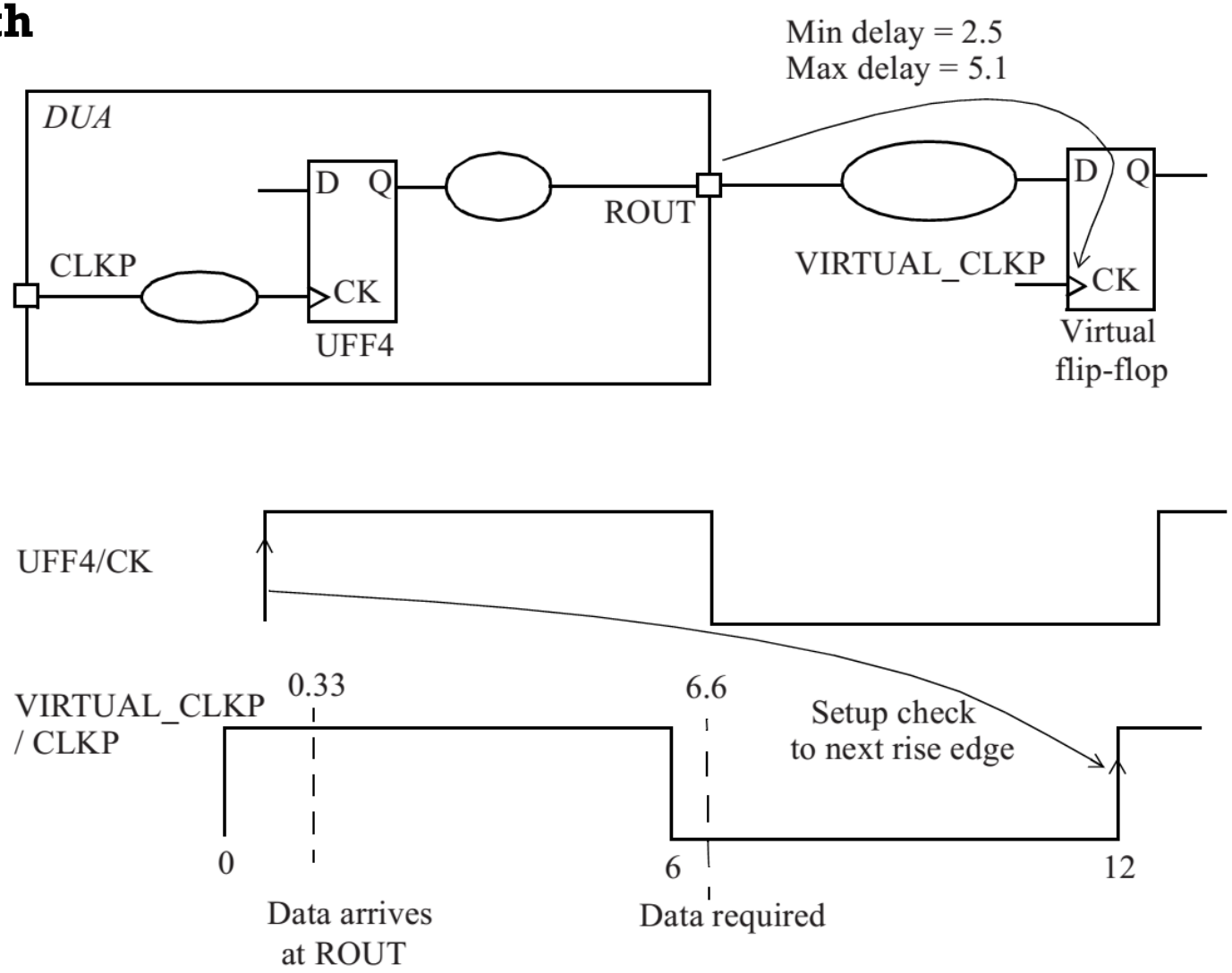
Setup Timing Check

3、Flip-flop to Output Path

```
set_output_delay -clock VIRTUAL_CLKP \
  -max 5.1 [get_ports ROUT]
set_load 0.02 [get_ports ROUT]
```

Setup Timing Check

3、Flip-flop to Output Path



Setup Timing Check

3、Flip-flop to Output Path

```
Startpoint: UFF4 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: ROUT (output port clocked by VIRTUAL_CLKP)
  Path Group: VIRTUAL_CLKP
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock CLKP (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKP (in)                                          0.00       0.00 r
  UCKBUF4/C (CKB  )                                  0.06       0.06 r
  UCKBUF5/C (CKB  )                                  0.06       0.12 r
  UFF4/CK (DFF )                                     0.00       0.12 r
  UFF4/Q (DFF )                                      0.13       0.25 r
  UBUF3/Z (BUFF  )                                   0.09       0.33 r
  ROUT (out)                                         0.00       0.33 r
  data arrival time                                             0.33
```

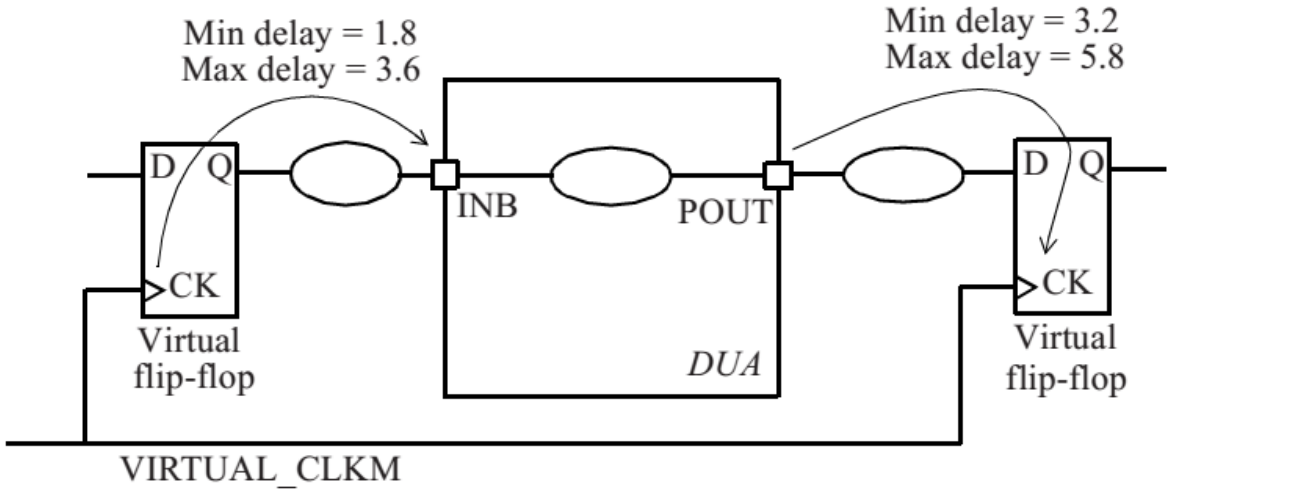
Setup Timing Check

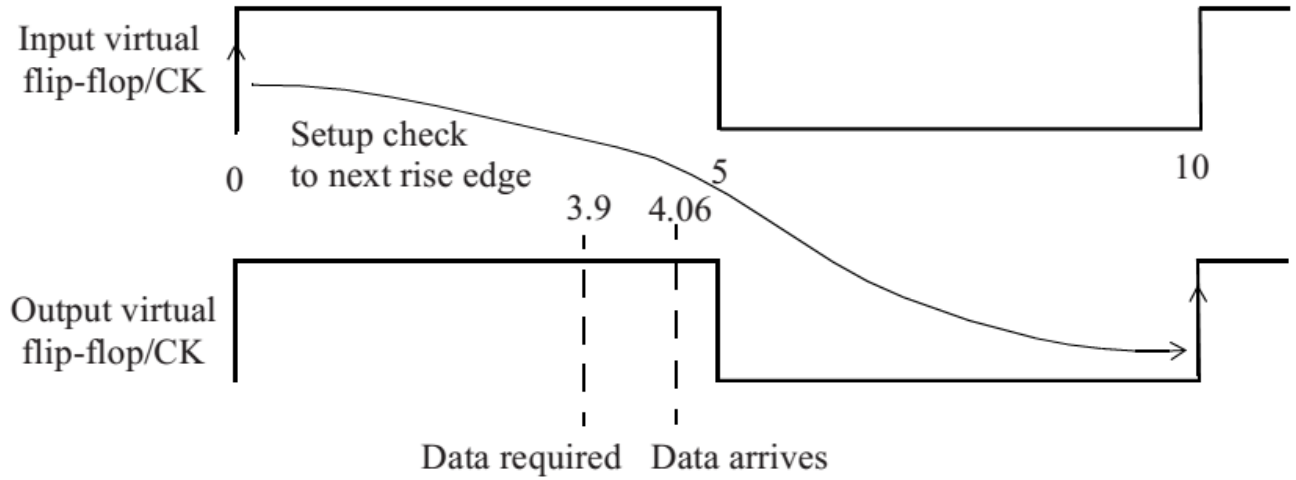
3、Flip-flop to Output Path

```
clock VIRTUAL_CLKP (rise edge)          12.00       12.00
clock network delay (ideal)              0.00       12.00
clock uncertainty                       -0.30       11.70
output external delay                   -5.10        6.60
-------------------------------------------------------------
data required time                                   6.60
data arrival time                                   -0.33
-------------------------------------------------------------
slack (MET)                                          6.27
```

Setup Timing Check

4、Input to Output Path





4、Input to Output Path

Here are the input and output delay specifications.

```
set_input_delay -clock VIRTUAL_CLKM \
  -max 3.6 [get_ports INB]
set_output_delay -clock VIRTUAL_CLKM \
  -max 5.8 [get_ports POUT]
```

Setup Timing Check

4、Input to Output Path

```
Startpoint: INB (input port clocked by VIRTUAL_CLKM)
Endpoint: POUT (output port clocked by VIRTUAL_CLKM)
Path Group: VIRTUAL_CLKM
Path Type: max

Point                                          Incr       Path
-----------------------------------------------------------------
clock VIRTUAL_CLKM (rise edge)                 0.00       0.00
clock network delay (ideal)                    0.00       0.00
```

Setup Timing Check

4、Input to Output Path

input external delay	**3.60**	3.60 f
INB (in) <-	0.00	3.60 f
UBUF0/Z (BUFF)	0.05	3.65 f
UBUF1/Z (BUFF)	0.06	3.72 f
UINV3/ZN (INV)	0.34	4.06 r
POUT (out)	0.00	4.06 r
data arrival time		4.06
clock VIRTUAL_CLKM (rise edge)	10.00	10.00
clock network delay (ideal)	0.00	10.00

Setup Timing Check

4、Input to Output Path

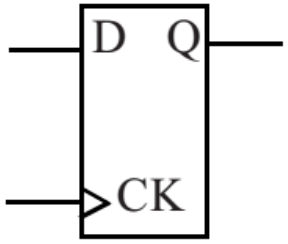
```
clock uncertainty                          -0.30        9.70
output external delay                      -5.80        3.90
data required time                                      3.90
-------------------------------------------------------------
data required time                                      3.90
data arrival time                                      -4.06
-------------------------------------------------------------
slack (VIOLATED)                                       -0.16
```

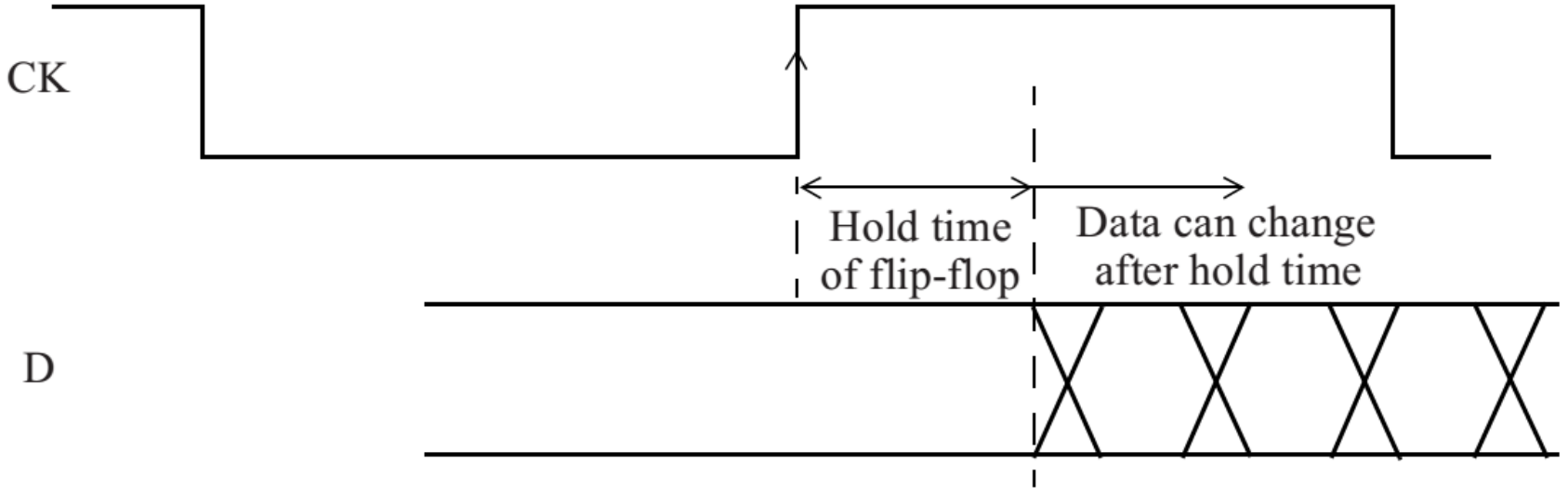
CONTENT

Part 5: Timing Verification

1. Setup timing check
2. Hold timing check

Hold Timing Check





Hold Timing Check

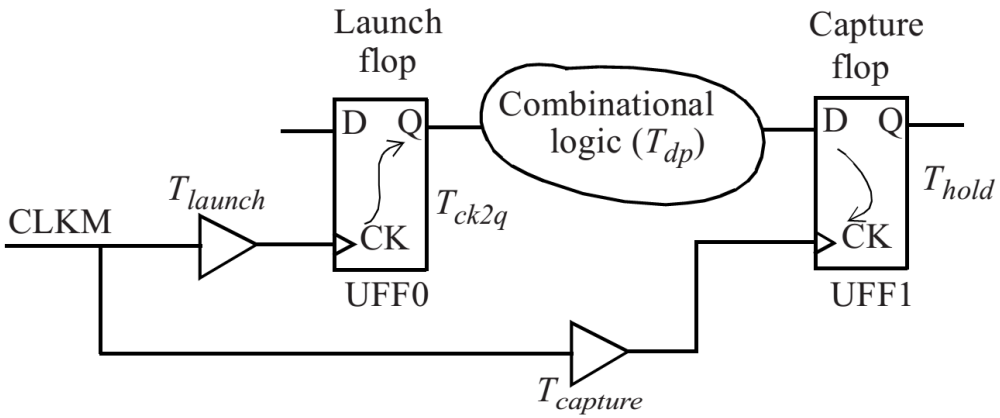
Just like the setup check, a hold timing check is between the launch flipflop - the flip-flop that launches the data, and the capture flip-flop - the flip-flop that captures the data and whose hold time must be satisfied.

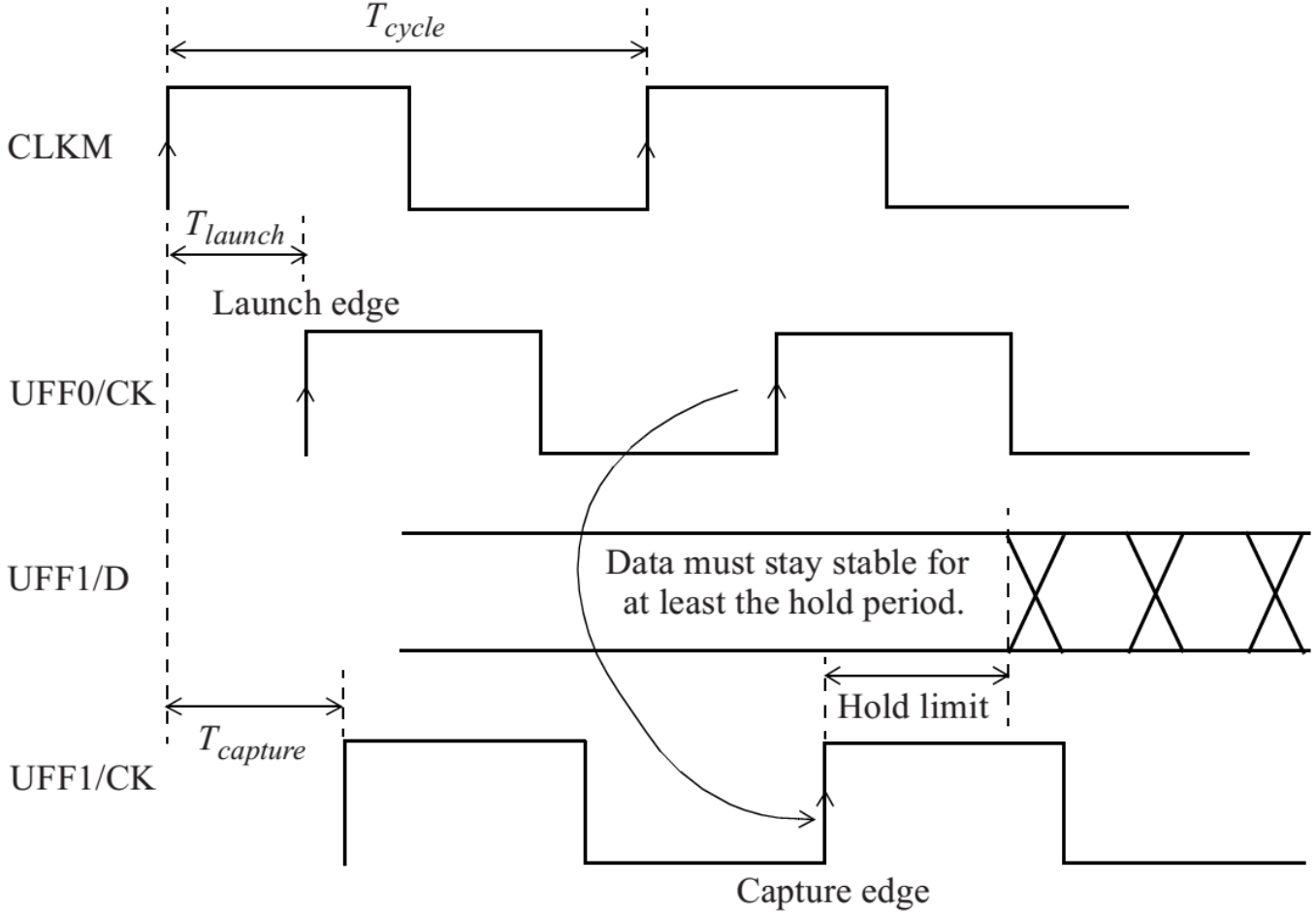
The clocks to these two flip-flops can be the same or can be different.

Hold Timing Check

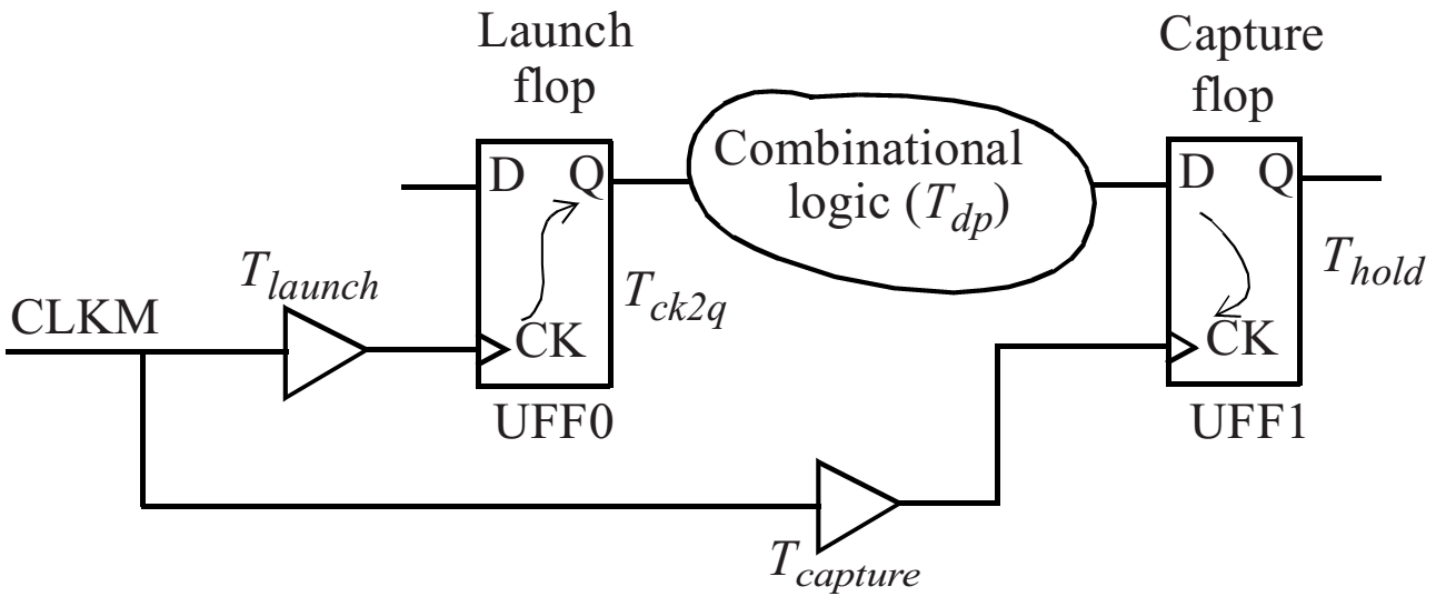
- The hold check is from one active edge of the clock in the launch flip-flop to **the same clock edge** at the capture flip-flop.
- Thus, a hold check is **independent** of the clock period.
- The hold check is carried out on each active edge of the clock of the capture flip-flop.

Hold Timing Check





Hold Timing Check



The hold check can be mathematically expressed as:

$$T_{launch} + T_{ck2q} + T_{dp} > T_{capture} + T_{hold}$$

Hold Timing Check

```
Startpoint: UFF0 (rising edge-triggered flip-flop clocked by CLKM)
  Endpoint: UFF1 (rising edge-triggered flip-flop clocked by CLKM)
  Path Group: CLKM
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------
  clock CLKM (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
  CLKM (in)                                          0.00       0.00 r
  UCKBUF0/C (CKB  )                                  0.06       0.06 r
  UCKBUF1/C (CKB  )                                  0.06       0.11 r
  UFF0/CK (DFF )                                     0.00       0.11 r
  UFF0/Q (DFF ) <-                                   0.14       0.26 r
  UNOR0/ZN (NR2  )                                   0.02       0.28 f
  UBUF4/Z (BUFF  )                                   0.06       0.33 f
  UFF1/D (DFF )                                      0.00       0.33 f
  data arrival time                                             0.33

  clock CLKM (rise edge)                             0.00       0.00
  clock source latency                               0.00       0.00
```

Hold Timing Check

CLKM (in)	0.00	0.00 r
UCKBUF0/C (CKB)	0.06	0.06 r
UCKBUF2/C (CKB)	0.07	0.12 r
UFF1/CK (DFF)	0.00	0.12 r
clock uncertainty	0.05	0.17
library hold time	**0.01**	0.19
data required time		0.19
data required time		0.19
data arrival time		-0.33
slack (MET)		0.14

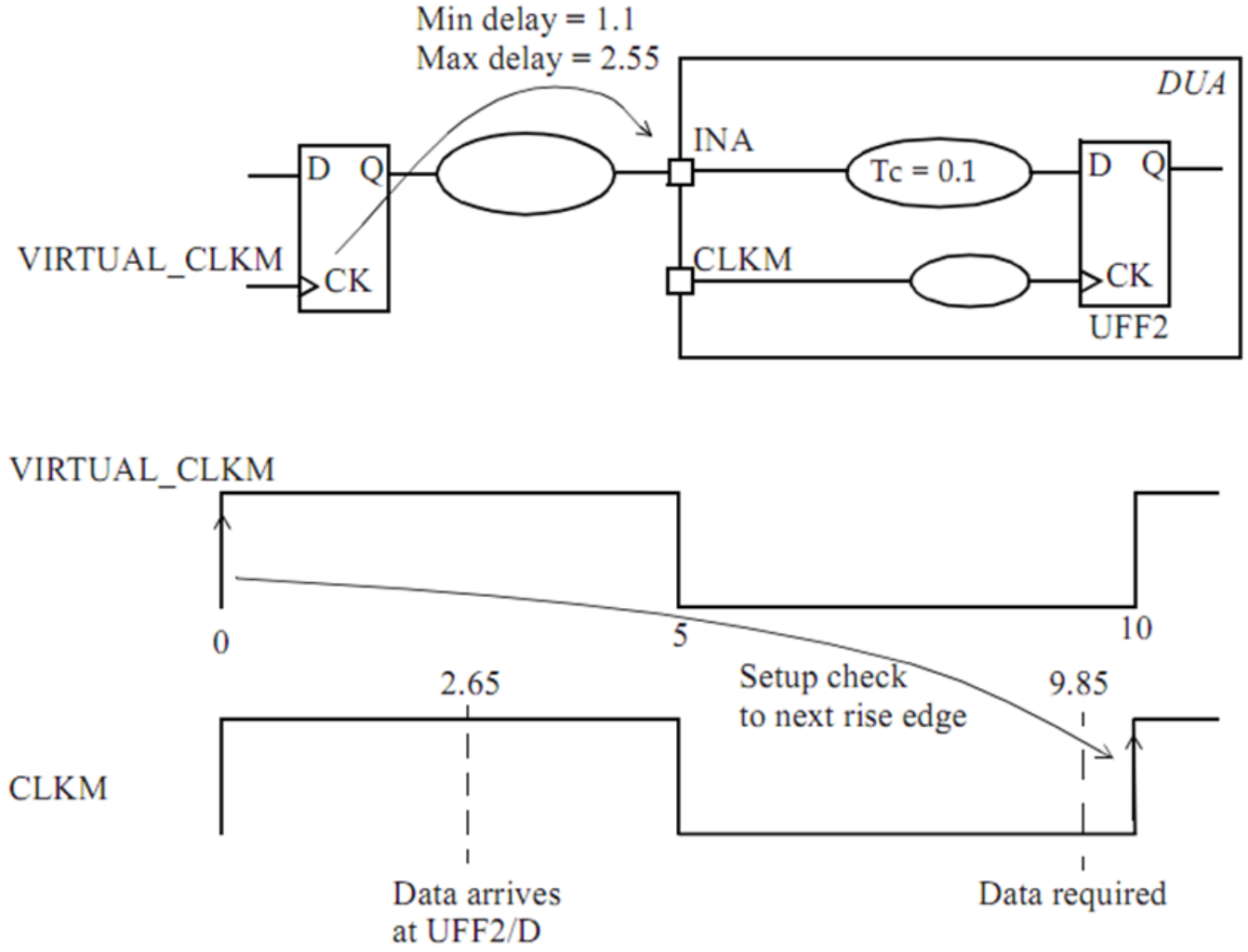
Hold Timing Check

Hold Slack Calculation:

- An interesting point to note is the difference in the way the slack is computed for setup and hold timing reports.
- In the setup timing reports, the arrival time and the required time are computed and the slack is computed to be the required time minus arrival time.

Hold Timing Check

1、Input to Flip-flop Path



set_input_delay -clock VIRTUAL_CLKM \ -min 1.1 [get_ports INA]

Hold Timing Check

Path Group: CLKM
Path Type: **min**

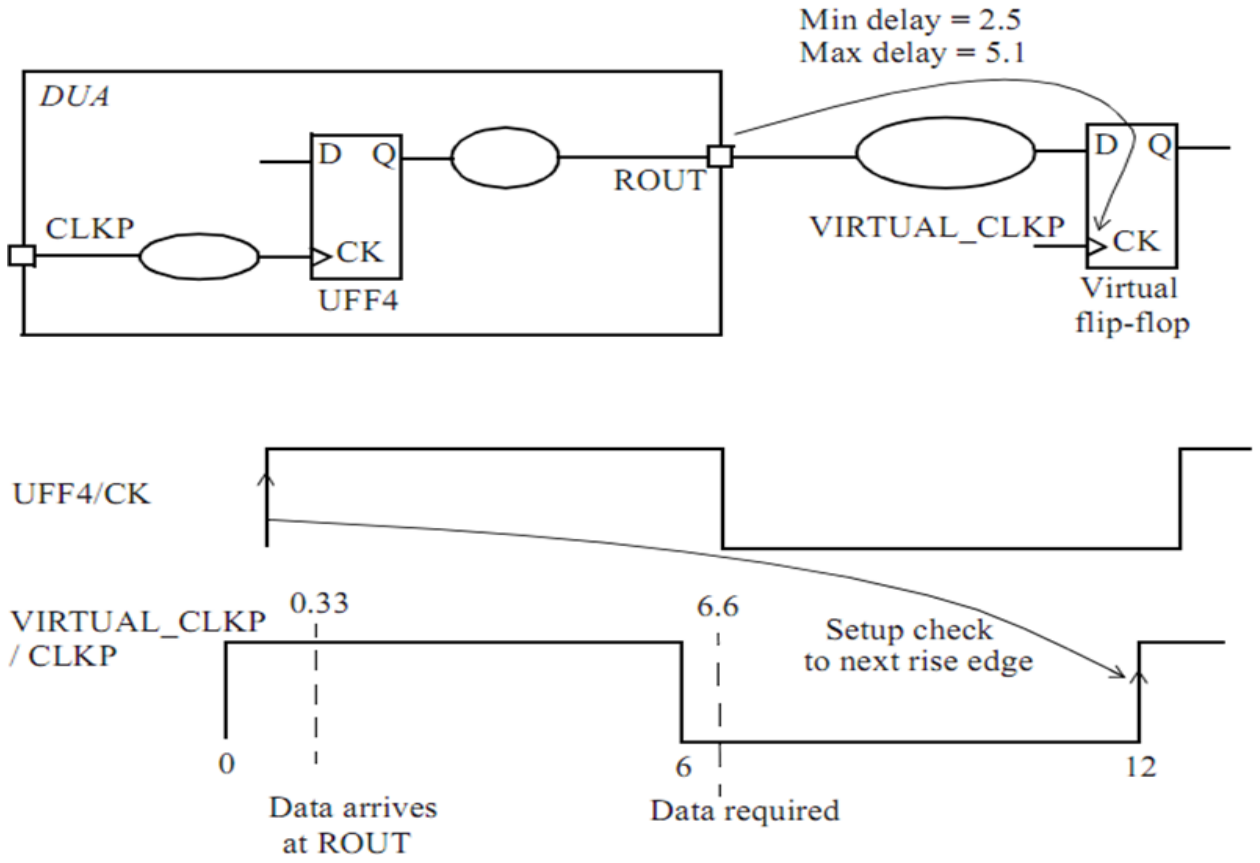
Point	Incr	Path
clock VIRTUAL_CLKM (rise edge)	**0.00**	0.00
clock network delay (ideal)	0.00	0.00
input external delay	**1.10**	1.10 f
INA (in) <-	0.00	1.10 f
UINV1/ZN (INV)	0.02	1.13 r
UAND0/Z (AN2)	0.06	1.18 r
UINV2/ZN (INV)	0.02	1.20 f
UFF2/D (DFF)	0.00	1.20 f
data arrival time		1.20

Hold Timing Check

clock CLKM (rise edge)	**0.00**	0.00	
clock source latency	0.00	0.00	
CLKM (in)	0.00	0.00	r
UCKBUF0/C (CKB)	0.06	0.06	r
UCKBUF2/C (CKB)	0.07	0.12	r
UCKBUF3/C (CKB)	0.06	0.18	r
UFF2/CK (DFF)	0.00	0.18	r
clock uncertainty	0.05	0.23	
library hold time	0.01	0.25	
data required time		0.25	
data required time		**0.25**	
data arrival time		**-1.20**	
slack (MET)		**0.95**	

Hold Timing Check

2、Flip-flop to Output Path



set_output_delay -clock VIRTUAL_CLKP \ -min 2.5 [get_ports ROUT]

Hold Timing Check

2、Flip-flop to Output Path

```
Startpoint: UFF4 (rising edge-triggered flip-flop clocked by CLKP)
  Endpoint: ROUT (output port clocked by VIRTUAL_CLKP)
  Path Group: VIRTUAL_CLKP
  Path Type: min

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLKP (rise edge)                   0.00       0.00
  clock source latency                     0.00       0.00
  CLKP (in)                                0.00       0.00 r
  UCKBUF4/C (CKB  )                        0.06       0.06 r
  UCKBUF5/C (CKB  )                        0.06       0.12 r
  UFF4/CK (DFF )                           0.00       0.12 r
  UFF4/Q (DFF )                            0.13       0.25 f
  UBUF3/Z (BUFF  )                         0.08       0.33 f
  ROUT (out)                               0.00       0.33 f
  data arrival time                                   0.33
```

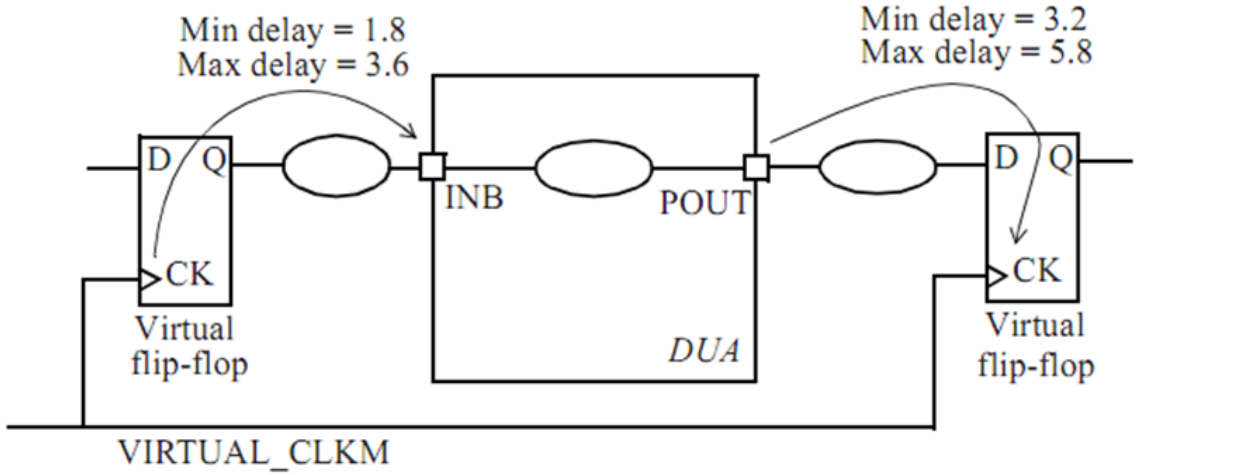
Hold Timing Check

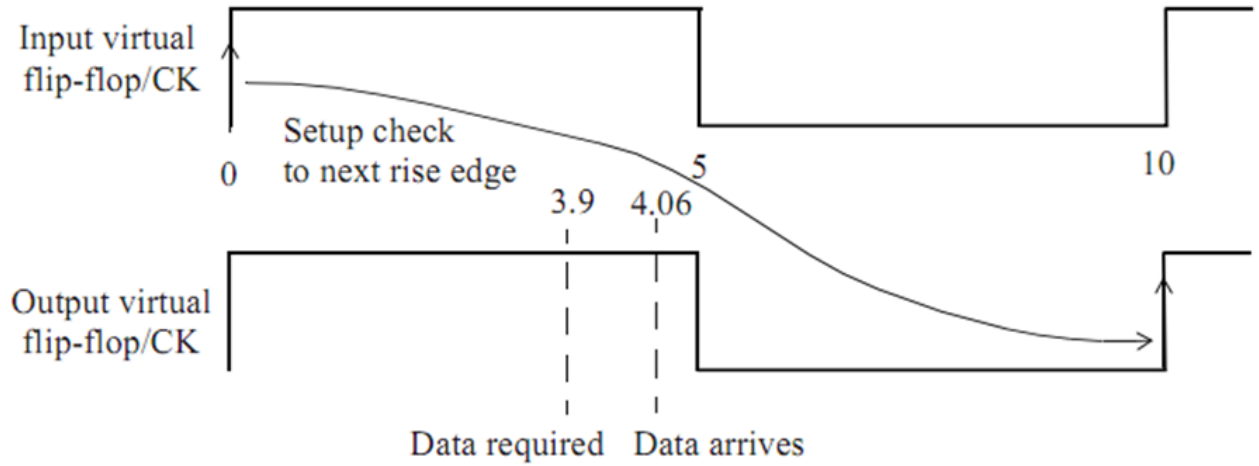
2、Flip-flop to Output Path

```
clock VIRTUAL_CLKP (rise edge)          0.00       0.00
clock network delay (ideal)             0.00       0.00
clock uncertainty                       0.05       0.05
output external delay                  -2.50      -2.45
data required time                                -2.45
-----------------------------------------------------------
data required time                                -2.45
data arrival time                                 -0.33
-----------------------------------------------------------
slack (MET)                                        2.78
```

Hold Timing Check

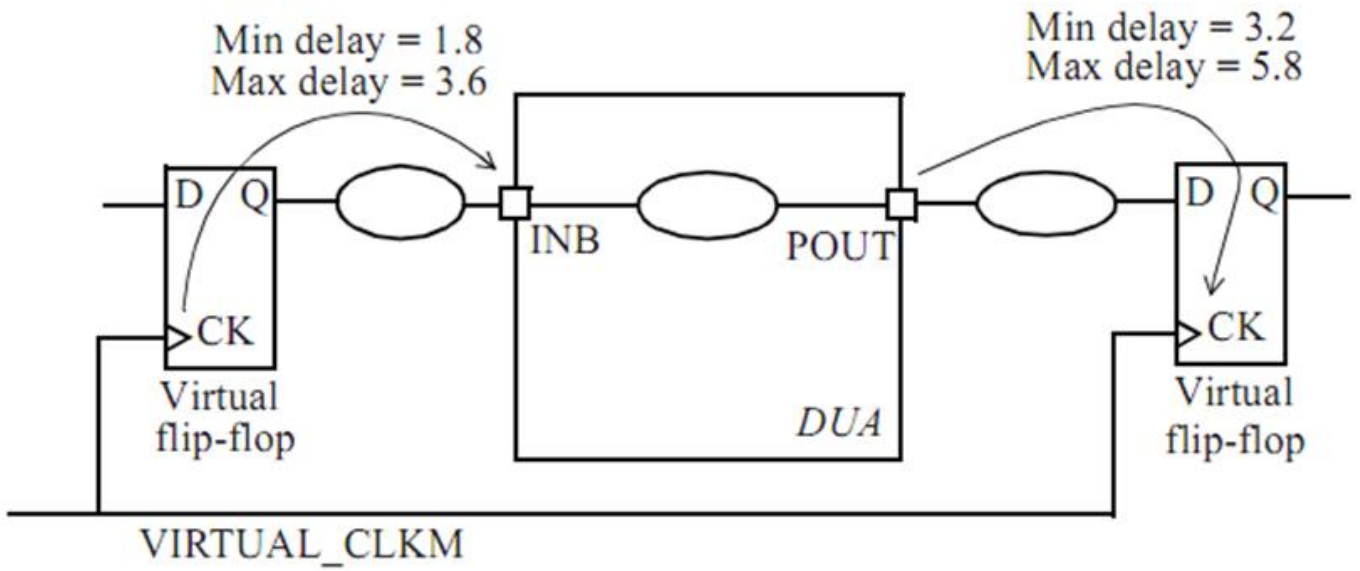
3、Input to Output Path





Hold Timing Check

3、Input to Output Path




```
set_load -pin_load 0.15 [get_ports POUT]
set_output_delay -clock VIRTUAL_CLKM \
  -min 3.2 [get_ports POUT]
set_input_delay -clock VIRTUAL_CLKM \
  -min 1.8 [get_ports INB]
set_input_transition 0.8 [get_ports INB]
```

Hold Timing Check

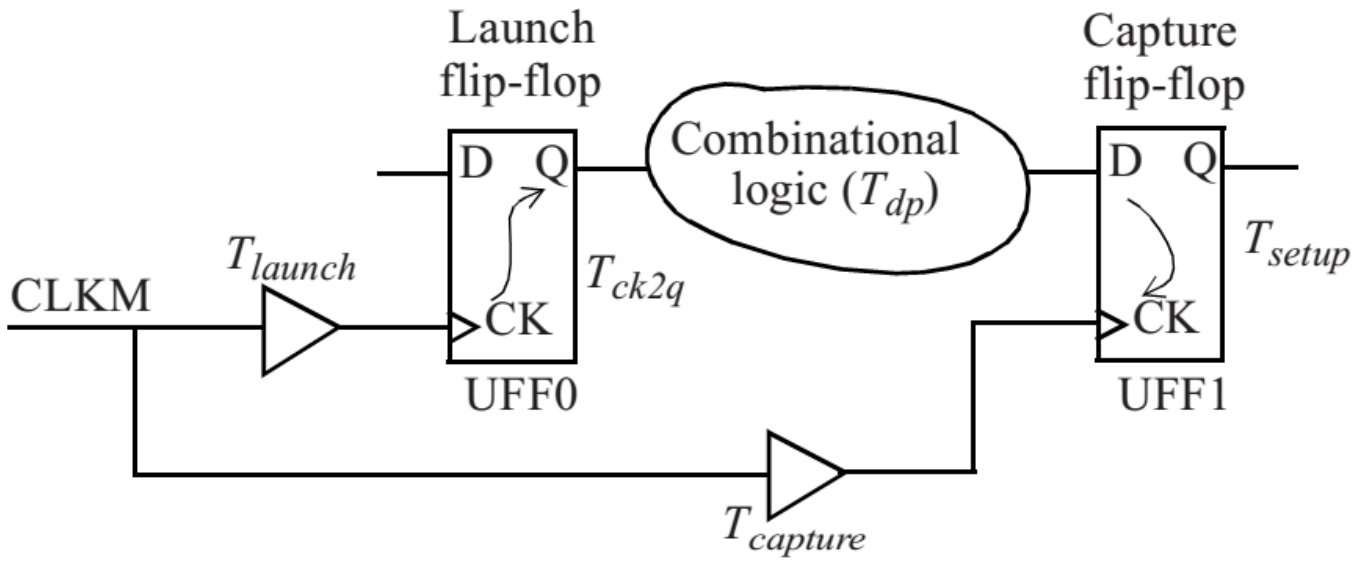
Startpoint: INB (**input port** clocked by VIRTUAL_CLKM)
Endpoint: POUT (**output port** clocked by VIRTUAL_CLKM)
Path Group: VIRTUAL_CLKM
Path Type: **min**

Point	Incr	Path
clock VIRTUAL_CLKM (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	**1.80**	1.80 r
INB (in) <-	0.00	1.80 r
UBUF0/Z (BUFF)	0.04	1.84 r
UBUF1/Z (BUFF)	0.06	1.90 r
UINV3/ZN (INV)	0.22	2.12 f
POUT (out)	0.00	2.12 f
data arrival time		2.12

Hold Timing Check

```
clock VIRTUAL_CLKM (rise edge)                0.00        0.00
clock network delay (ideal)                   0.00        0.00
clock uncertainty                             0.05        0.05
output external delay                        -3.20       -3.15
data required time                                       -3.15
-------------------------------------------------------------
data required time                                       -3.15
data arrival time                                        -2.12
-------------------------------------------------------------
slack (MET)                                               5.27
```

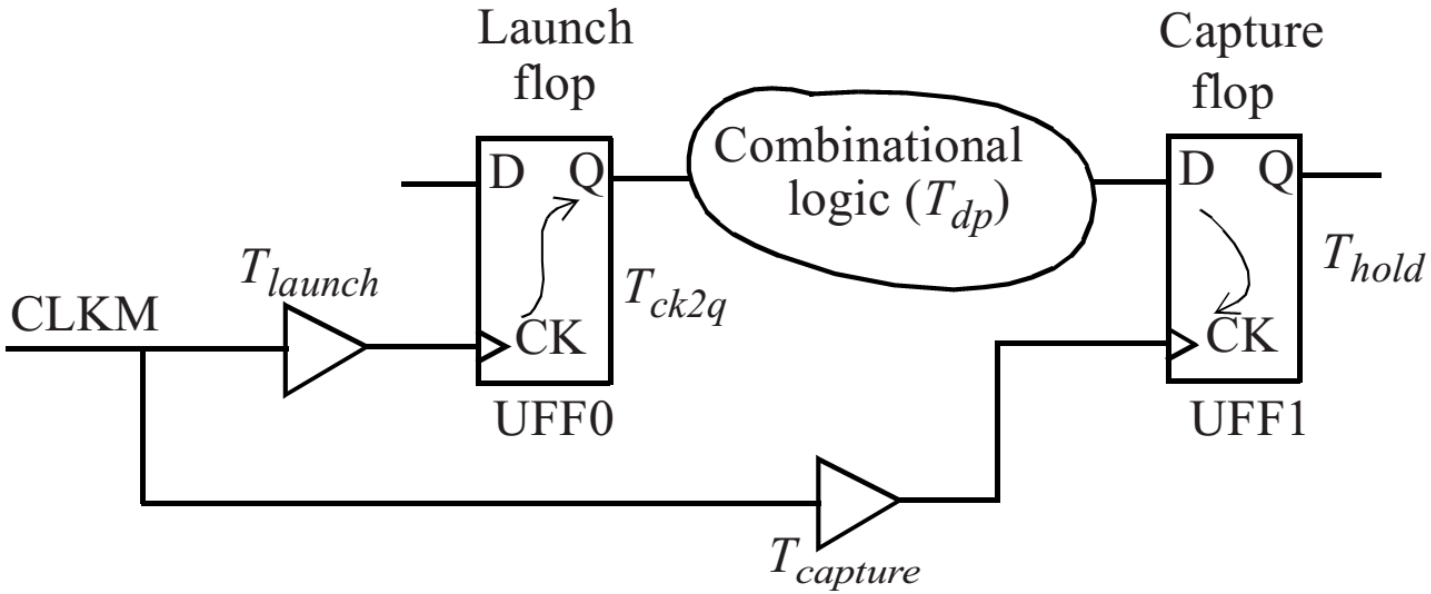
Conclusion-Setup Timing Check



The setup check can be mathematically expressed as:

$$T_{launch} + T_{ck2q} + T_{dp} < T_{capture} + T_{cycle} - T_{setup}$$

Conclusion-Hold Timing Check



The hold check can be mathematically expressed as:

$$T_{launch} + T_{ck2q} + T_{dp} > T_{capture} + T_{hold}$$

参考书目

- Static Timing Analysis for Nanometer Designs: A Practical Approach. J. Bhasker, Rakesh Chadha. Springer Science Business Media, LLC 2009. Chaper 7.
- 集成电路静态时序分析与建模. 刘峰，机械工业出版社.出版时间：2016-07-01. 第六章.

谢谢聆听！

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