VeriSilicon

Written Test - A
SOC Design
(Exam duration: 60min)

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Signature: [redacted]

Home Address: 西安市雁塔区太白南路2号.

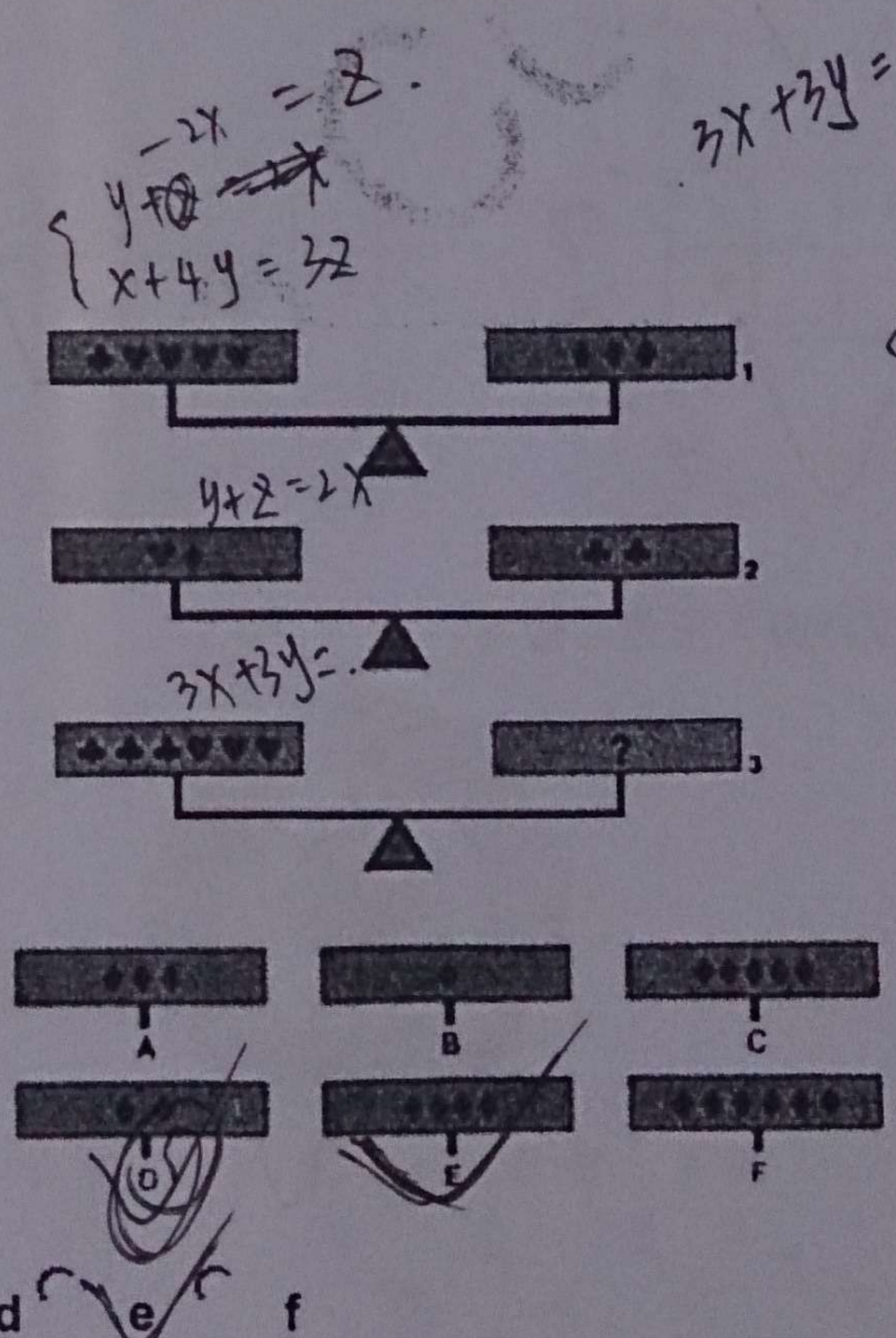
Please select the type of your diploma: ☐Master of Science ☑Master of Engineering

Note

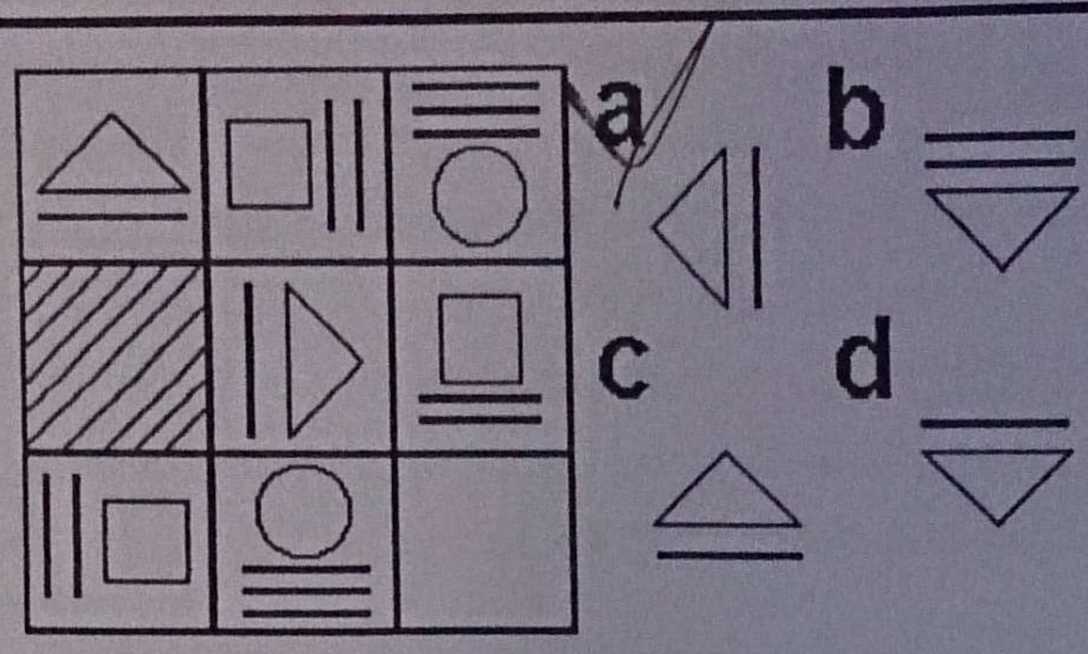
1. The answers can be written in English or Chinese.
2. The exam paper must be handed back before you leave.

I. IQ

1.

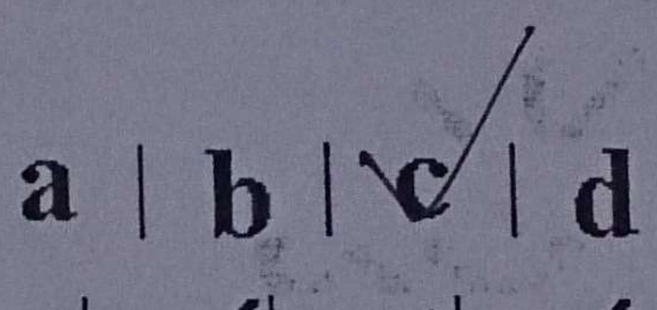


2. 请从右边的图形中选择一个正确的(a,b,c,d)填入左边的空白：

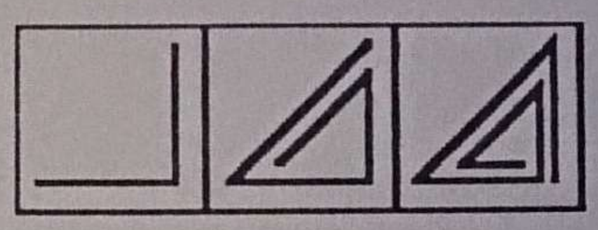


a b c d

3. 在下列题目中每一行都缺少一个图，请从右边选择一个(a b c d)插入左边图形中以使左边的图形逻辑角度上能成双配对：

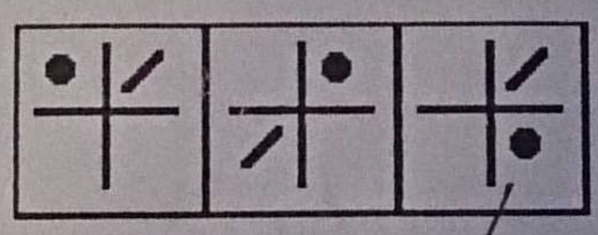


1)



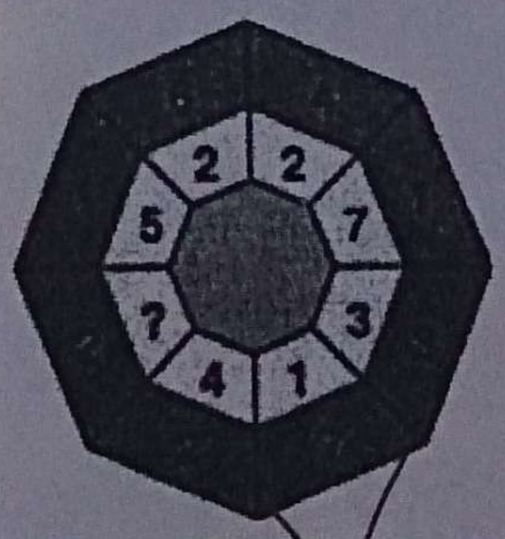
a b c d

2)



a b c d

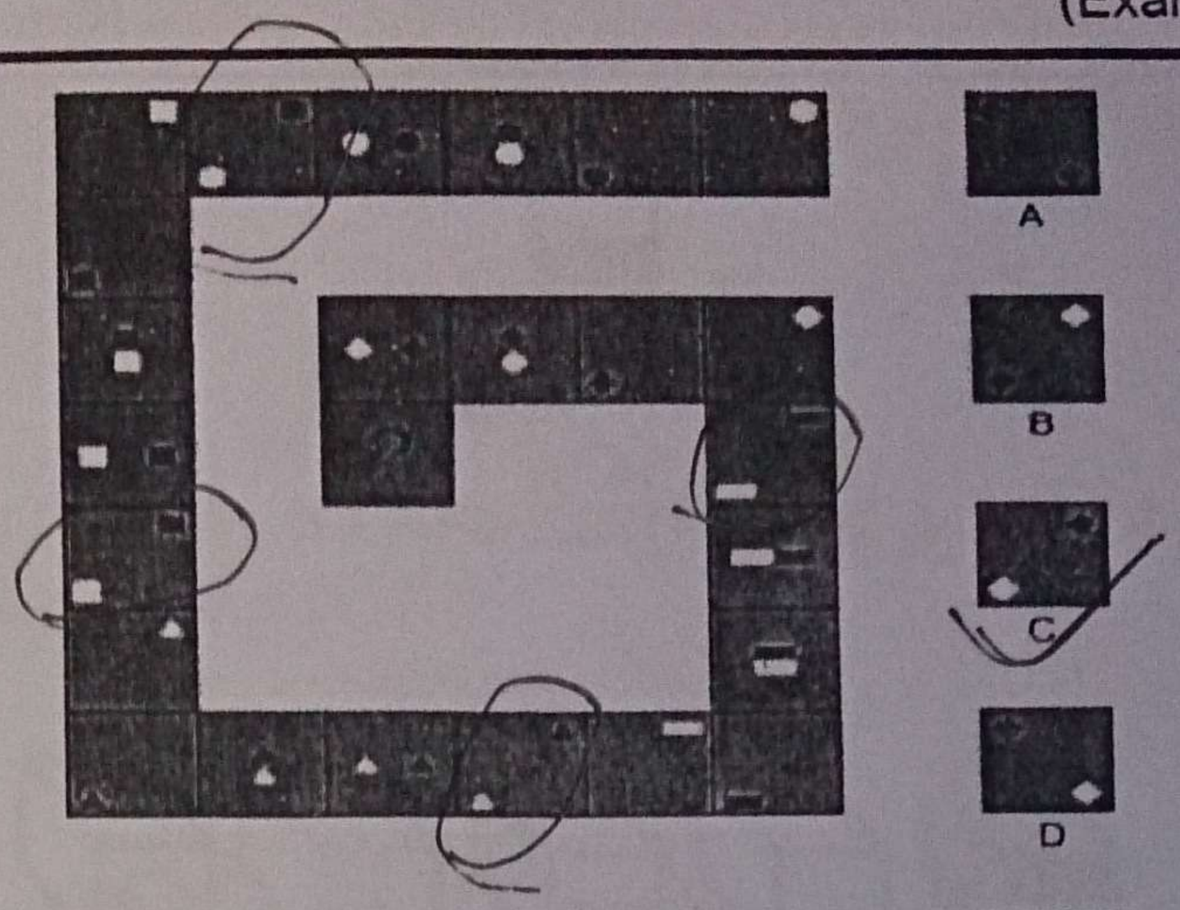
4. 请从逻辑或理论角度推算？所需的数字：



A: 1 B: 5 C: 4 D: 6 E: 9 F: 8

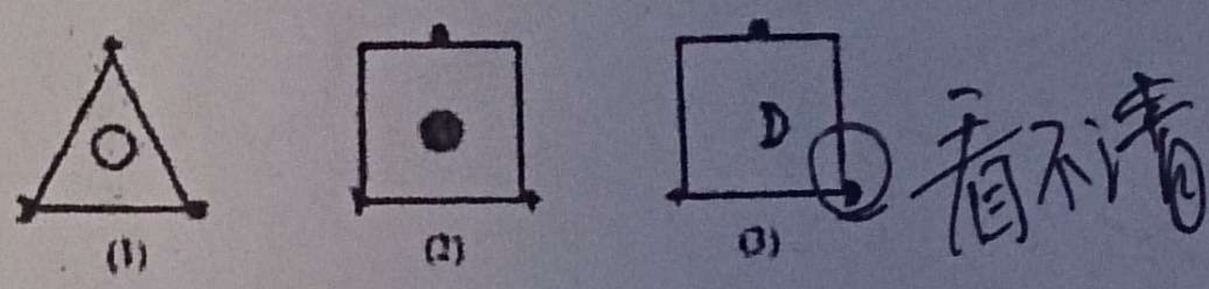
a b c d e f

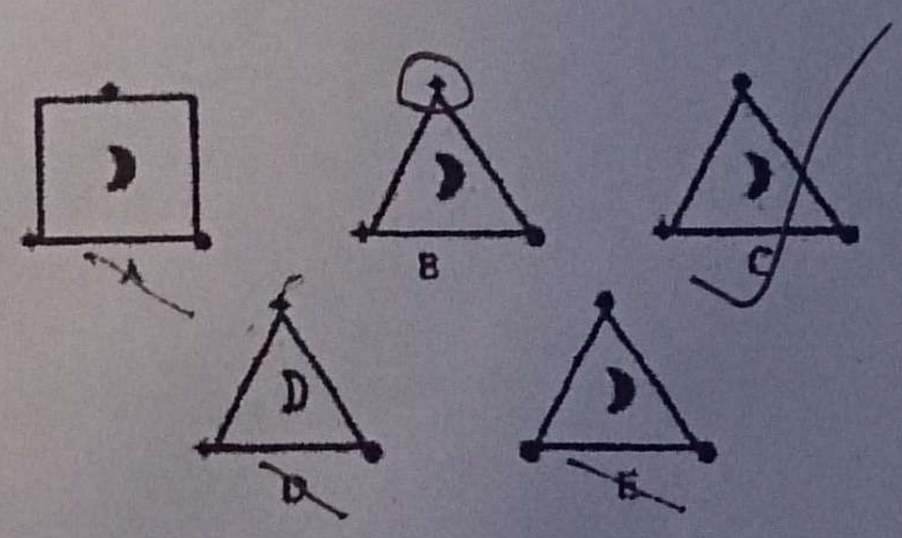
5. 请从逻辑或理论角度推算？所需的图片：



a b c d e f

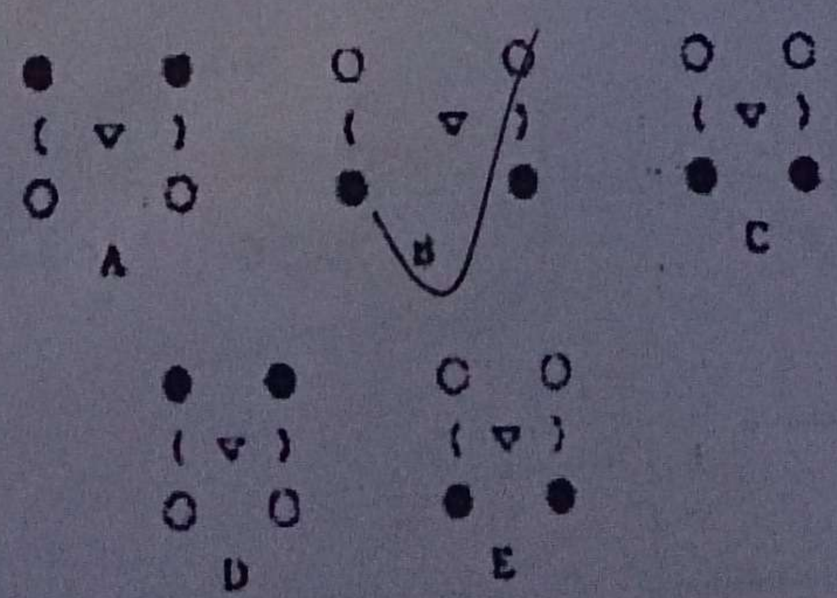
6. 根据（1）和（2）的逻辑关系，（3）和下面那一个图形相似?





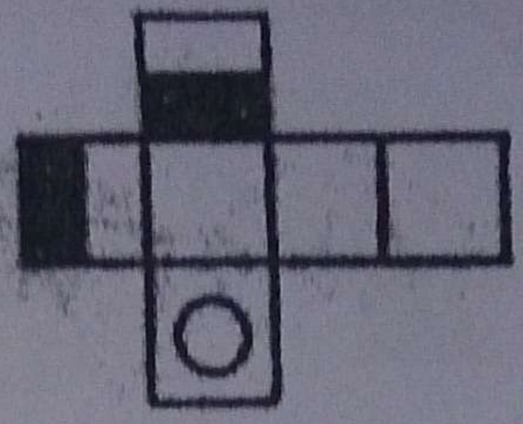
a b c d e

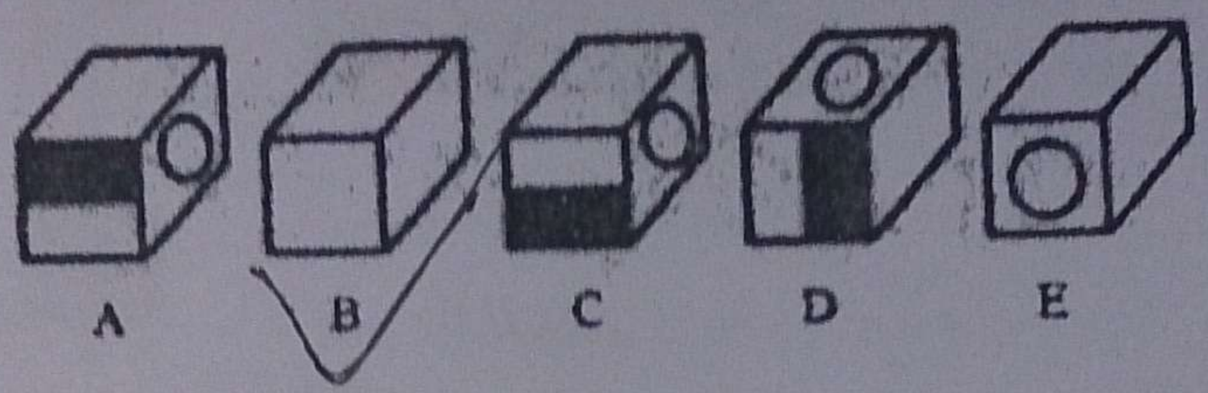
7. 下列图形哪一个不同于其他图形?



a b c d e

8.将下面的图形折成正方体，不可能形成哪个图形？



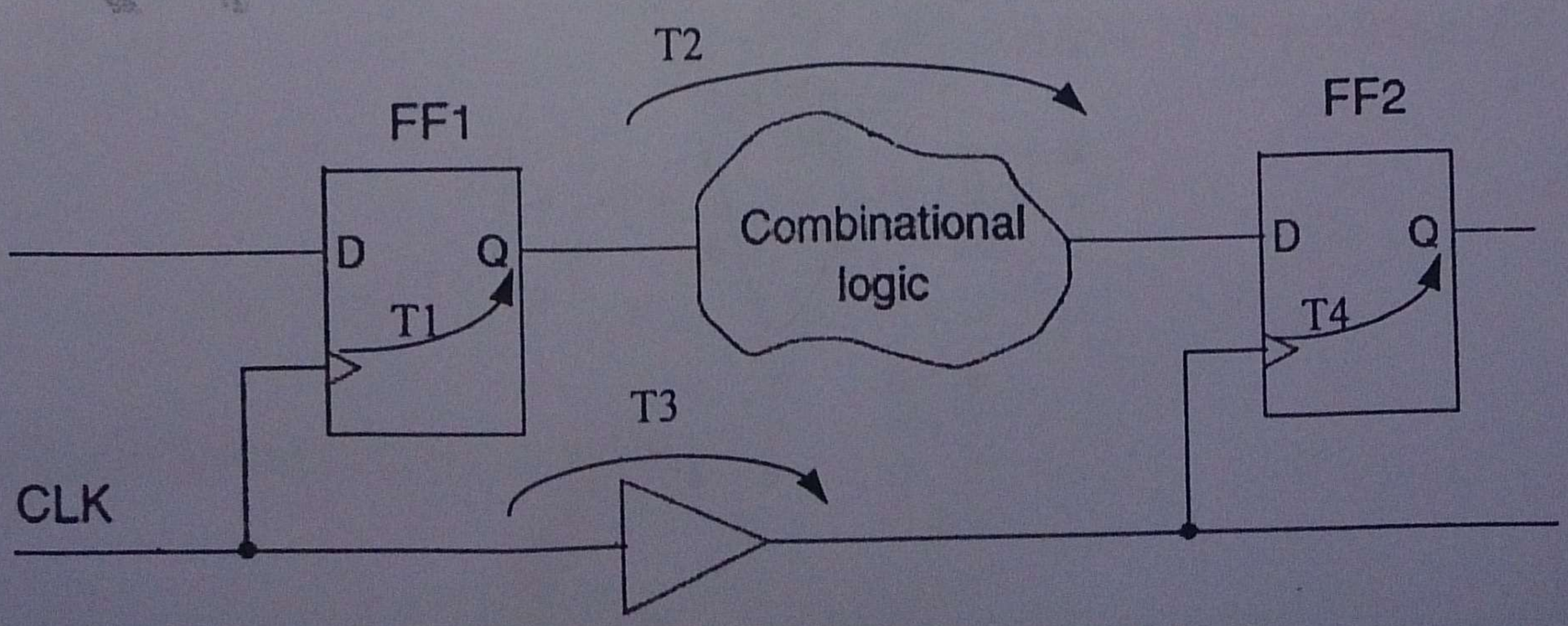


(a (b (c (d (e

II. IC Basic Knowledge Related Questions

1. Please describe the ASIC design flow from SPEC to GDSII.

2. Please explain the setup and hold check, by using T1, T2, T3, T4 and clock period T0.



$T_1 + T_2 \leq T_3 + T_0 - T_{setup}$.

$T_{setup} \leq T_3 + T_0 - T_1 - T_2$

$T_1 + T_2 - T_3 \geq T_{hold}$

3. Please explain the basic difference between X86 series and MPIS/ARM; please explain the basic pipeline of CPU.

III. Design/Verification/SoC Questions (choose ≥ 4 questions to answer)

1. Please list how to reduce power in the entire ASIC design flow from SPEC to GDSII

2. How to take care of single-bit signals from different clock domain? What about multi-bits signals?

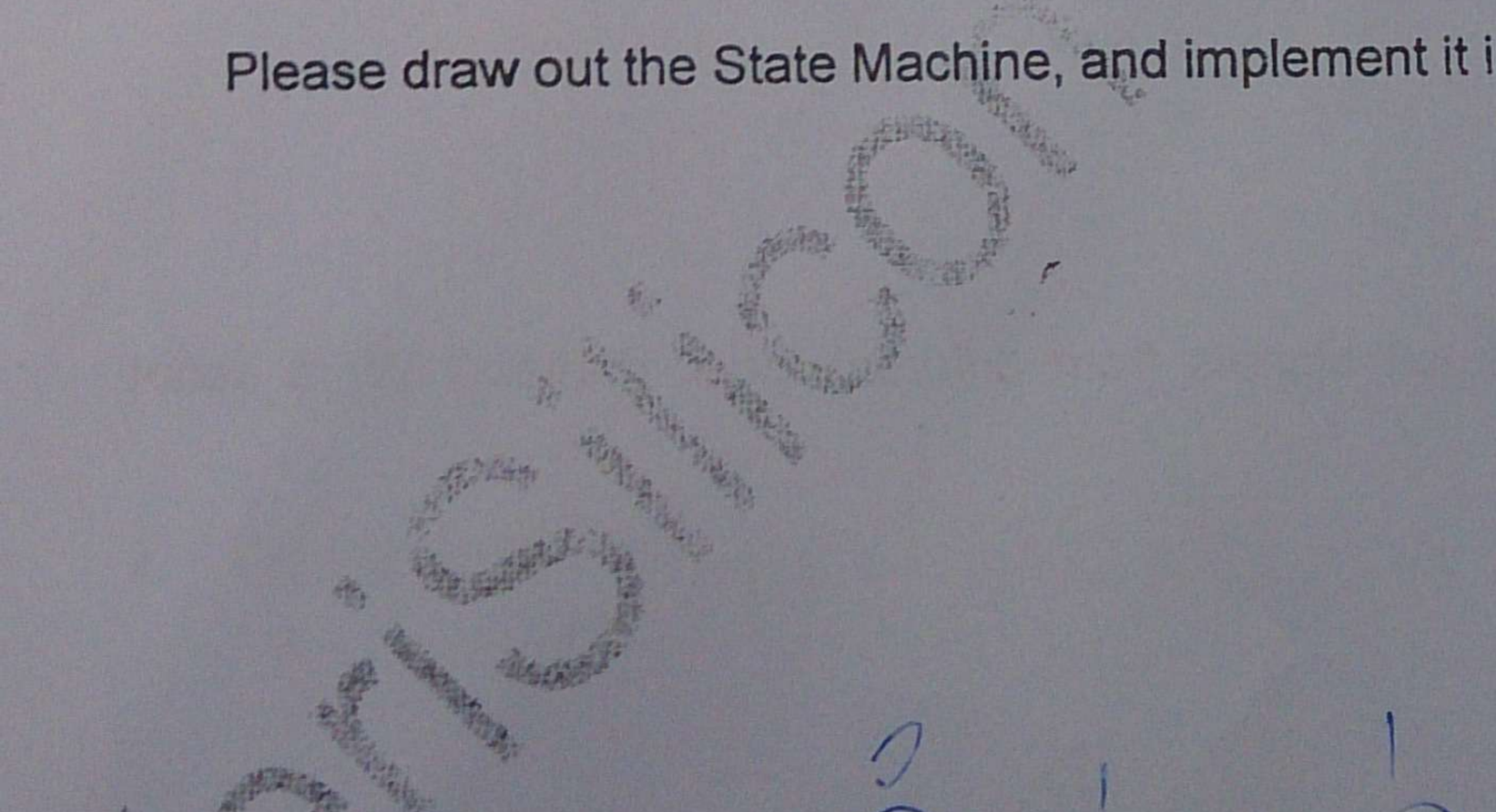
3. Please explain why DRAM requires periodically refresh but SRAM not; please explain what is CAS latency, Addictive latency, and the relationship between read latency and these two latencies.

4. Please design a module to detect serial data sequence "1001" from input port "x". When serial sequence "1001" is detected, the output port "z" becomes "1", otherwise be "0". For example,

   x: 000 101 010 010 011 101 001 110 101

   z: 000 000 000 010 010 000 001 000 000

Please draw out the State Machine, and implement it in Verilog/VHDL.



5. Please explain a) basic idea of DFT; b) the difference between a scan DFF and a basic DFF; and c) why should scan DFF be used?

6. Please illustrate differences among the video formats: Y'CbCr4:2:0, Y'CbCr 4:2:2, Y'CbCr 4:4:4.

7. What is entropy coding? Use CABAC as an example to describe the steps to coding a data symbol.