I. Flow/Timing/DFT Related Questions: Please select at lease 5 questions to answer

Here is a timing report from Primetime.

Startpoint: FF1 (falling edge-triggered flip-flop clocked by Clk)

Endpoint: FF2 (rising edge-triggered flip-flop clocked by Clk)

Path Group: Clk

Path Type: min

Point	Incr	Path
clock Clk (fall edge)	2.00	2.00
clock network delay (propagated)	0.90*	2.90
FF1/CLK (fdmf1a15)	0.00	2.90 f
FF1/Q (fdef1a15)	0.40*	3.30 f
U2/Y (buf1a27)	0.05*	3.35 f
U3/Y (buf1a27)	0.05 #	3.40 f
FF2/D (fdef1a15)	0. 01*	3.41 f
data arrival time		3.41
clock Clk (rise edge)	0.00	0.00
clock network delay (propagated)	1.00*	1.00
FF2/CLK (fdef1a15)		1.00 r
library hold time	0.10*	1.10
data required time		1.10
data required time		1.10
data arrival time		-3.41
slack (MET)		2.31

1) Try to draw a schematic of this timing path.

2) The timing path is_____•

a. synchronous path b- asynchronous path c. can’t be determined

3) The timing report is _____•

a. setup timing report b. hold timing report c. can’t be determined

4) The timing shows the path_____ .

a. violates timing requirement b. meets timing requirement, c. can’t be determined

5) The timing report is_____.

a. pre-layout timing report b. post-layout timing report c. can’t be determined

6) The clock frequency is _____ MHz if the duty cycle is 50%. The clock uncertainty is _____ ns.

7) The operating condition is_____•

a. worst b. typical c. best d. unknown

8) What's test risk? Please fix the risk and draw the schematic.

2. The power gating cell reduces _____•

a. dynamic power b. static power c. leakage power d. all of above

3. The isolation cell isolates _____••

a. paths from high voltage to lower voltage domains.

b. paths from lower voltage to higher voltage domains.

c. paths from turn-on to turn-off domains.

d. paths from turn-off to turn-on domains.

e. paths from higher frequency to lower frequency dock domains.

f. paths from lower frequency to higher frequency clock domains.

4. What are the key factors of power consumption of a design?

5. What's the difference between noise and xtalk of digital design?

6. List the basic pins for normal scan test. Draw the waveform while testing according to the pin you listed