

III. APR Questions : Please select at least 3 questions to answer

1. In VLSI chip design we need many STD cells/IO/Memory and IPs which include more than GDS/CD, to achieve the VLSI design, what else information do we need?
2. In a VLSI chip, what's the relationship between R/C loading and metal layer width/length; and the relationship between R/C loading and gate delay?
3. In a VLSI chip there are many clock trees, please try to explain the clock tree relationship between the two modes: normal operation mode and testing mode.
4. What is IR drop, what is OCV?
5. What's the signal EM? How to fix it?